Performance Analysis of Gigabit Ethernet Standard for Various Physical Media Using Triple Speed Ethernet IP Core on FPGA

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Abstract. Gigabit Ethernet Standard provides 1 Gbps bandwidth and is backward compatible with 10 Mbps (Ethernet) and 100 Mbps (Fast Ethernet). It can also be installed with lower cost than other technologies having similar speed. The performance studies of Gigabit Ethernet is more complex than Ethernet or Fast Ethernet protocols. In this paper we have described the implementation of Gigabit Ethernet design on FPGA using Altera's Triple Speed Ethernet IP Core. The performance analysis of Gigabit Ethernet Standard has been studied using various physical media. This analysis includes performance measurements with different number of frames and frame lengths.

Keywords: MAC, Triple Speed Ethernet, Gigabit Ethernet, SFP.

1 Introduction

Software-based programmable network interfaces excel in their ability to implement various services.[1] These services can be added or removed in the network interface simply by upgrading the code in the system. However, programmable network interfaces suffer from instruction processing overhead. Programmable NICs must spend time executing instructions to run their software whereas ASIC (Application Specific Integrated Circuit) based network interfaces implement their functions directly in hardware. To address these issues, an intelligent, configurable network interface is an effective solution. A reconfigurable NIC (Network Interface Card) allows rapid prototyping of new system architectures for network interfaces. The architectures can be verified in real environment, and potential implementation bottlenecks can be identified. Architecturally, the platform must be processor-based and must be largely implemented using a configurable hardware. Thus, an FPGA (Field Programmable Gate Array) with an embedded processor can be the best platform to combine performance, efficiency and versatility. Dynamically reconfigurable platform will also reduce power consumption of the network device [2].Also, the reconfigurable NIC must have different memory interfaces including high capacity memory and high speed memory for adding new networking services.

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2 Gigabit Ethernet Standard

Figure 1 presents a block diagram identifying the various components of IEEE Std 802.3z.The media access control (MAC) sublayer describes the algorithms used to control the transmission and reception of frames on an Ethernet network. IEEE Std 802.3z includes both the full duplex MAC and the carrier sense multiple access with collision detection (CSMA/CD) MAC [3]. The gigabit media-independent interface (GMII) allows any physical layer to be attached to the MAC and thus provide interoperability between different vendors. The GMII delivers 8-bit octets to the physical coding sublayer (PCS) on the transmit path, and accepts 8-bit octets from the PCS on the receive path at a rate of 125 million octets (1 billion bits) per second. The 10-bit symbols produced by the PCS are serialized by the physical medium attachment (PMA) sublayer. The PCS includes a function referred to as auto negotiation, which is a link startup and initialization procedure. Within IEEE Std 802.3z, auto negotiation is used to select between the CSMA/CD and full duplex operating modes, and to select whether the Pause flow control mechanism is enabled or disabled on a link-by-link basis.

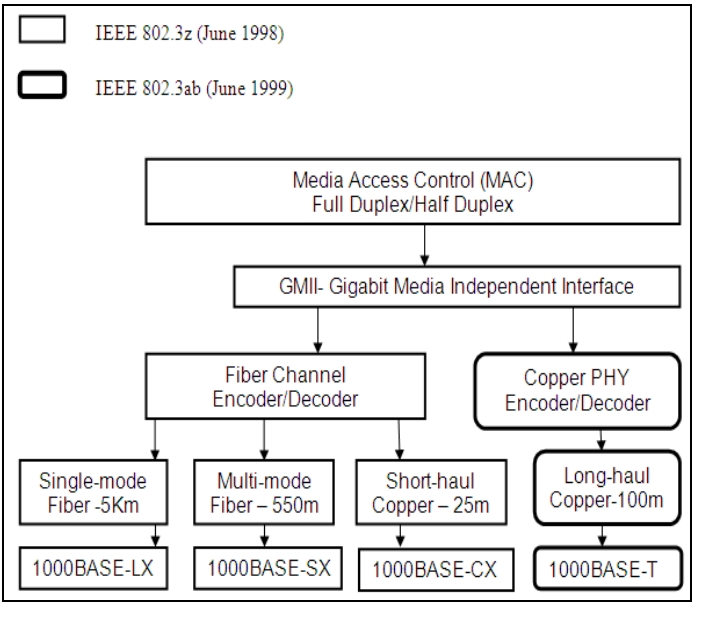

Fig. 1. Gigabit Ethernet Standard [3]

The transceiver specifications are given at the bottom of the diagram.The 1000BASE-SX specification for short-wavelength laser transceivers supports multi-mode fiber optic links at distances up to 275 m using 62.5 μ fiber, and 550 m using 50 μ fiber. 1000BASE-LX supports longer distances using higher-cost components, spanning 550 m on 62.5 μ or 50 μ fiber, and up to 5 km on single-mode fiber. The

1000BASE-LX laser transmitter is optimized for single-mode fiber, and requires a mode-conditioning patch cord to support multimode fiber optic cable. Both 1000BASE-SX and 1000BASE-LX specify the familiar duplex SC optical connector, eliminating the most common installation problem encountered in fiber optic networks, the misconnection of the transmitting and receiving fibers. IEEE Std 802.3z also includes a specification for a transceiver technology referred to as 1000BASE-CX, which supports shielded copper cables links spanning 25 m. The SerDes component which makes up the PMA sublayer is designed to drive this cable directly, which makes 1000BASE-CX an economically attractive choice for short-distance interconnections, for instance, between devices located within the same rack or within a computer room or telephone closet. 1000BASE-T supports 1000 Mb/s operation on four pairs of category 5 UTP cabling, at a maximum link distance of 100 m. A 1000BASE-T PHY transmits its signal on all four pairs of wire simultaneously, thus reducing the data rate on each pair to 250 Mbps. The use of a five-level pulse amplitude modulation scheme further reduces the signaling rate on each pair. Hybrids and digital echo cancellation are used to achieve full-duplex communication.

3 System Organization

Fig.2 shows a high-level block diagram of the Triple Speed Ethernet (TSE) design[4]. The design includes two Altera TSE MegaCore functions (MAC + PCS + PMA) and is downloaded on Altera's Stratix II GX PCI Express Development Kit. There are two SFP(Small Form-factor Pluggable) cages built onto the kit. This design interfaces the TSE MegaCore function[5] with a Copper or Optical Fibre SFP module via a 1.25 Gbps serial transceiver that enables all 10, 100, and 1000 Mbps Ethernet operations. The design sends stream of Ethernet packets to the TSE MegaCore function, which can be looped back using SFP modules with an Ethernet fibre optic cable, copper cable or a switch.The design can demonstrate the operation of the TSE MegaCore function in various modes with live traffic upto the maximum throughput rate and show the error rate in the receiver, if any.

The design is built using Altera's Quartus II software and SOPC (System On Programmable Chip) builder .The Nios II processor is used as a control plane component for setting up and configuring the system components. The Ethernet packets are generated and monitored by the processor.The on-chip memory is of block size 256 Kbytes, which is used for storage of software code.The parallel input/output (PIO) core provides easy I/O access to the 1000BASE-T Copper or Optical Fibre SFP module's PHY registers.The JTAG UART core transfers serial character streams between a Nios II processor and an SOPC Builder system.The phase-locked loop (PLL) core takes an input clock from a 100 MHz crystal on the development kit and generates an 83.33 MHz PLL output clock as a system-wide clock source for the SOPC Builder system.The TSE Megacore function transmits the Ethernet packets from the Avalon Streaming (Avalon-ST) interface to a 1.25 Gbps serial transceiver interface that is built in the Stratix II GX device and receives packets from the opposite direction.The Ethernet Packet Generator is an SOPC custom component, used to generate a stream of Ethernet packets.It drives the Transmit FIFO interface of TSE MegaCore

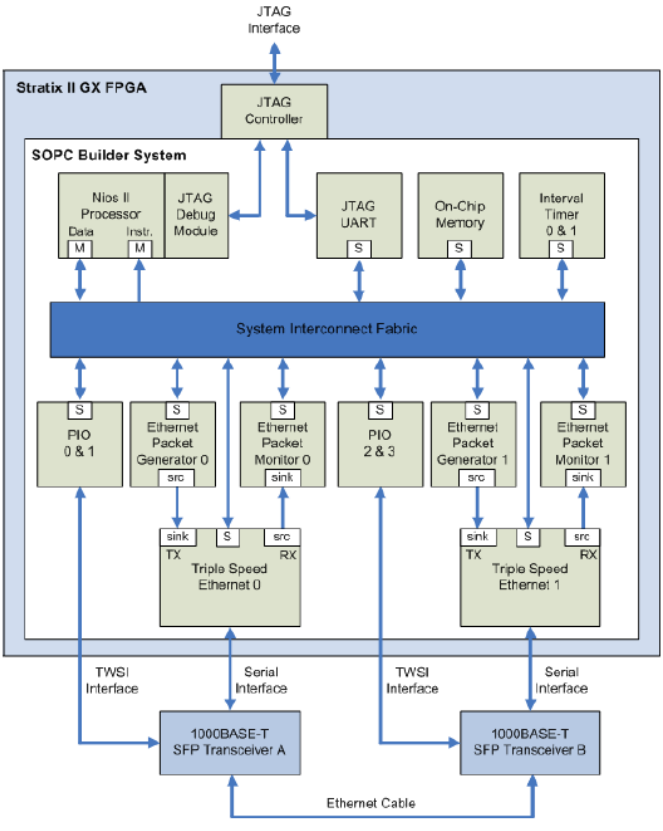

Fig. 2. Block Diagram of Triple Speed Ethernet Reference Design [4]

function. The Ethernet Packet Monitor block is an SOPC custom component created using the component editor. It has an Avalon-MM slave interface on one side for control purposes and an Avalon-ST sink interface on the other side for the data path. This block is fed a stream of Ethernet packets by the TSE MegaCore function Receive FIFO interface. The Ethernet Packet Monitor also verifies the accuracy of the received payload.The interval timer core is a 32-bit timer used by the Nios II processor system to calculate the performance and throughput rate of various Ethernet operations.

4 Implementation

Altera's Triple Speed Ethernet Design has been used as a platform for studying the performance of Gigabit Ethernet Standards 1000Base-LX, 1000Base-SX and 1000Base-T. The design has been implemented on Altera's Stratix II GX device EP2SGX90FF1508C3.Table 1 summarizes the utilization result of this design.

Table 1. Resource Utilisation of Triple Speed Ethernet Design

Parameter	Value	Utilization(%))
Logic	15281	21
Combinational ALUTs	11209	15
Dedicated logic registers	10419	14
Total pins	32	4
Total block memory bits	390494	9
DSP block 9-bit elements	8	2
Total PLLs	1	13
Total GXB Receiver Channels	2	13
Total GXB Transmitter Channels	2	13

5 Performance Evaluation and Results

The network performance instrument with measuring ability of full line rate is an important component of the system[6].The Test System of the Ethernet design is given below in Fig.3. The Triple Speed Ethernet design is dumped onto the FPGA using Quartus II software and JTAG interface.

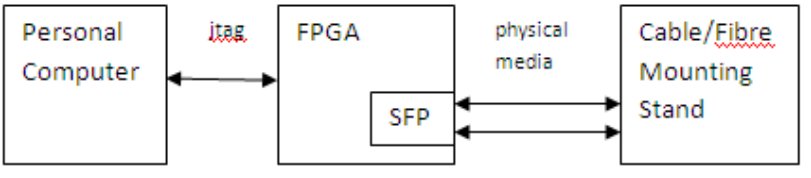

Fig. 3. Test System for Performance Evaluation

The performance of above design was studied for Gigabit Ethernet standards 1000Base-LX ,1000Base-SX and 1000Base-T using various physical media and corresponding SFP Transceivers as mentioned in Table 2.

Table 2. List of SFP Transceivers used for the different Gigabit Ethernet standards

Sr. No.	SFP Transceiver	Physical media	Gigabit Ethernet Standard
1	1000Base-LX 1310nm	Singlemode Fibre (SMF)	1000Base-LX
2	1000Base-LX Bi-Di 1310nm, 1550nm	Singlemode Fibre (SMF)	1000Base-LX
3	1000Base-SX 850nm	Multimode Fibre (MMF)	1000Base-SX
4	1000BaseT	Cat-5e	1000Base-T

The system was tested by varying parameters such as message length and number of frames .The first test was performed by increasing the message length and keeping the number of frames fixed . The test was repeated for two different values of number of frames i.e. 10^5 and 10^7 . The results of the tests performed for all the Gigabit Ethernet Standards mentioned in Table 2 is given in Table 3. It is found that as the message length is increased from 64 bytes to 9600 bytes, the line rate increases and achieves 99.79% for 9600 bytes. The throughput is 1488115 packets per second(pps) for 64 bytes and 12993 pps for 9600 bytes.The results are found to be nearly the same for all the different Gigabit standards.

Table 3. Throughput of the Network

Length (bytes)	Line rate (%)	Throughput (pps)
64	76.19	1488115
128	86.48	844607
256	92.75	452905
512	96.24	234966
1024	98.08	119733
1518	98.70	81275
2048	99.03	60445
4096	99.51	30369
8192	99.75	15221
9600	99.79	12993

The second test was performed for the different Gigabit Ethernet standards by varying message length from 64 bytes to 9600 bytes and measuring Line rate and Throughput. From the Figure 4 and Figure 5, it can be seen that the curves for the 3 standards 1000Base-LX ,1000Base-SX and 1000Base-T almost overlap. Hence the performance of the 3 standards are found to be almost similar. This measurement was taken for fixed number of packets 10^5 and 10^7.

The third test was performed by keeping the total number of bytes (N) sent constant.N =message length×number of packets .The message length was varied from 64 bytes to 9600 bytes and correspondingly number of packets was changed.The experiment was repeated for 2 different values of N i.e. 64×10^5 and 64×10^7. Fig.6 shows that the throughput is the same for both values of N for a particular message length. Fig.7 shows that the line rate obtained is same for both values of N for a particular message length.Also the values of Line rate and Throughput are the same as in Table 3 (where number of frames is kept fixed). The Total transmission time(t) has reduced from .067s for 64 bytes message length to .051s for 9600 bytes when N= 64×10^5 as shown in Fig.8. Similarly, as the message length is increased , t is reduced from 6.72s to 5.13s for N=64×10^7 as illustrated in Fig.9.

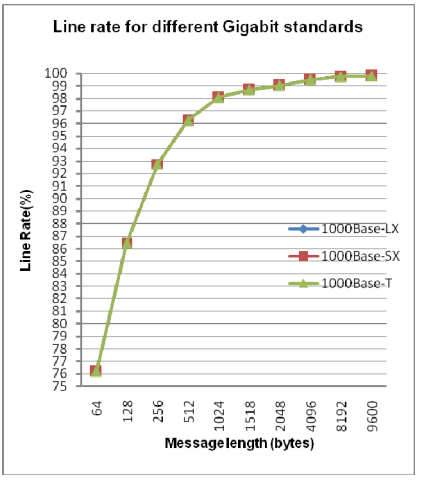

Fig. 4. Line rate vs. message length

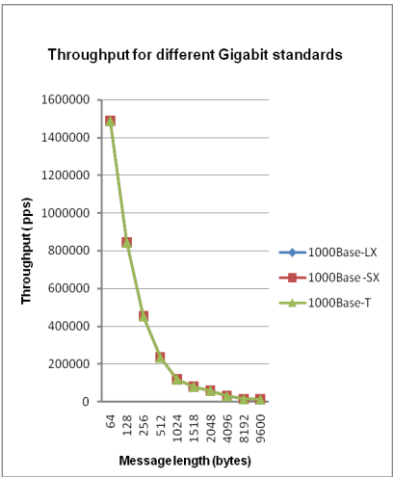

Fig. 5. Throughput vs. message length

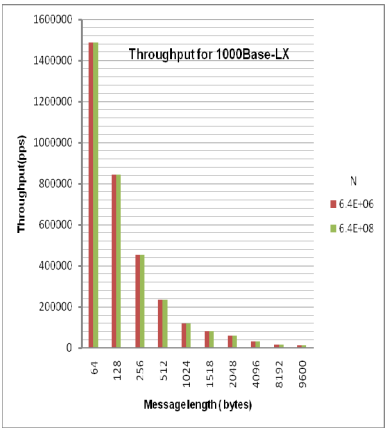

Fig. 6. Throughput vs. message length

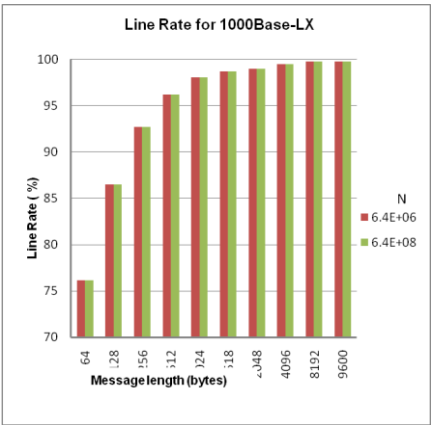

Fig. 7. Line rate vs. message length

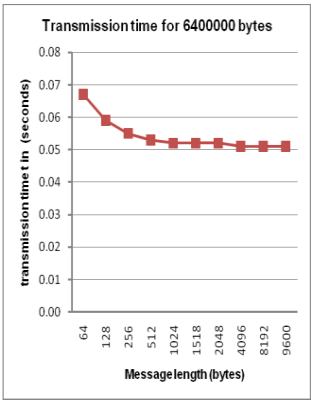

Fig. 8. Transmission time vs. message length

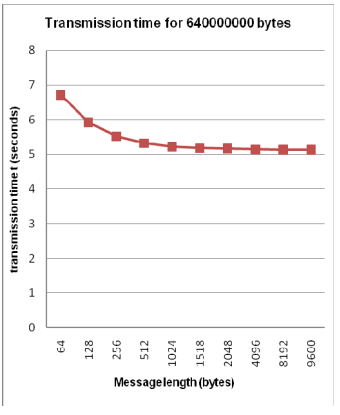

Fig. 9. Transmission time vs. message length

This test was performed only for 1000Base-LX standard and similar performance is expected of the other standards. The use of SOPC has given us the flexibility to choose from different software and hardware components and greatly reduce the system development cycle[7].

6 Conclusion and Future work

This paper has studied the performance analysis of Gigabit Ethernet Standards, implemented on Altera's FPGA. Quartus II software is used to synthesize and create .sof file .The design is downloaded to the FPGA chip using JTAG interface.Experimental results reveal that the line rate is 76.19% for minimum 64 bytes packet size and approaches 100% for 9600 bytes packet size.The throughput is lowest for 64 bytes packet size and increases with increase in packet size.for various packet lengths .For a particular packet size, the throughput and line rate remain almost the same for all the different Gigabit Ethernet standards. Also, as the packet length increases , the total transmission time is found to be decreasing.We have also developed an experimental platform to introduce errors into the network and future work includes Error Detection and Correction Analysis using the same platform.

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