Network On Chip Performance Analysis Over 2-D and 3D Mesh Topologies For CBR & FTP Applications

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Abstract— **Network on Chip (NoC) is an approach to designing the communication subsystem between IP cores in a System on a Chip (SoC).Numerous topologies with various capacities have been proposed for NoCs, various topologies and parameters are chosen based on different NoC applications. In this paper, we have modeled the 2DMesh topology for 16X16,2D Torus 16x16 and 3D 18x18 nodes for varying packets size (0.1 and 16000Kbytes), queue size(5-200), link bandwidth(10-200Mbps), link propagation delay(10-200ms), over CBR(5 and 10Mbps) and FTP applications. This paper presents the design of a scalable packet based router allowing data transfer and managing dynamically several communications in parallel. The performance of throughput and propagation delay of packets from given source node to destination node is studied for low(0.512Kbytes) and high load(64Kbytes) applications. Point by point similar investigation of the reproduction brings about terms of latency and throughput are displayed. The outcomes can be utilized as a rule for NoC architects to settle on fitting decisions keeping in mind the end goal to accomplish ideal execution for respective applications of future wireless communications systems is to provide sensor data transmission high-data-rate,quality of service (QoS),low cost,speed of wireless access .**

Index Terms—**NoC(Network on Chip); SoC(System on Chip);Mesh Topology, Verification.**

I. INTRODUCTION

Nowadays design paradigms of highly complex and integrated system on chip are based on the assembling of predesigned cores and components (Intellectual property, IP cores). NoC is an efficient on chip communication architecture for SoC architectures that is reusable, high performance, integration of a large number of computational, scalable and storage blocks on a single chip. Network on Chip is characterized by routing algorithm, topology and switching technique.

Tremendous developments in VLSI technology as per International Technology and Roadmap for Semi-conductors (ITRS), the Integrated Circuit (IC) productions organizations started producing single silicon chips with thousand billion integrated transistors each, utilizing nano-meter design [1]. This allows integration of thousands of homogenous and heterogeneous parts together to give full usefulness of an application on a single chip called System on Chip (SoC). When there are thousands of homogenous or heterogeneous Intellectual Property (IPs), the communication between various IP blocks become the focus of designing high performance and reliable SoC[2-3]. With great deal of IPs, the bus and point-to-point technology; clearly it'll cause a high value, as well as interconnect delay, power consumption and traffic collision. Likewise conventional transport based interconnect structures can't scale adequately past a specific number of imparting assets, consequently, turning into a bottleneck toward the billion transistor chip [2]. To adapt to the wastefulness of transports, VLSI analysts, concocted a novel packet based interconnect design for future SoCs - Network on Chip (NoC). The thinking is to relate various resources on a chip through a framework where correspondence happens using groups rather than interfacing the advantages by method for dedicated wires.

NoC has been proposed as a highly structured and scalable solution to address communication problems in SoC. On chip interconnection network provides advantages over dedicated wiring and buses, i.e. low-latency, low-power consumption and scalability. Each resource should be contacted to a switch in the network via a network interface (NI). More topologies have been discussed for this switch network includes 2D Mesh, Folded Torus, Ring, Butterfly Fat Tree, Octagon and irregular connection net-works. The most of place efficient ones on a 2D Mesh and binary tree [4]. There is favorable position in work topology [7] as it has its own particular manner of steering called source directing. This component in this topology gives a proficient encoding of way data with just few bits. Obviously every jump is adequately encoded with just two bits. As the bundle which is entering the switch is sustained with a pre-characterized choice about the goal port, outlining of switch is made fundamentally basic. Since the header is made with just couple of bits, the plan is basic and additionally the system not reliant with the size.
This paper presents the study and design of a NoC topology with different topologies: 2D-mesh and 2D-torus,3D-mesh. The basic element of this topology is a switch making possible the communication between the IPs cores.

This paper organized to first section introduction of NoC, Second section discuss the state of art NoC technology, and third section modeling of the proposed mesh topology, introduced different topologies, discuss the results analysis. At last fourth stage is the discussion and conclusion of proposed system.

II. LITERATURE SURVEY AND STATE OF THE ART IN NoC

Some related works for the parking space management system based on wireless sensor networks are reviewed in this.

Many researchers are found proposing demonstration of NoC in simulating environment in analytical and simulation based model in 2 & 3-dimensions for various types of topologies like as mentioned above. Topologies such as mesh, torus, octagon, SPIN, BFT etc. were analyzed for performance i.e. delay parameters [8]. Source directing i.e. the source hub decides just its neighboring hubs that are included in message conveyance is utilized for work topology. For the situation of Octagon, embrace the various leveled address-based directing. BFT, CLICHE, and Folded Torus give bring down throughput than SPIN and Octagon.The 2D work and 2D torus interconnection systems has been assessed, where they actualized both with and without affirmation instrument and parcels has been sent utilizing uniform movement design. Comes about demonstrate that, the torus has a decent execution and quick when affirmation instrument is utilized and work perform better when without affirmation component is utilized[9][11].

Jin-xiang Wang et al. [12] have described a new fault model, defines separately node-fault and link-fault, reduces situations classified as node-fault effectively and consequently improves the performance of the network. By defining some new paths to substitute failure paths, data packets can be routed along the new paths which are formed by the neighbor nodes of node-fault or link-fault. A fault-tolerant wormhole router based on XY routing algorithm is designed according to the solution. The evaluation results show that network performance can be improved by 15% when link-fault occurs in the network. Hamed S. Kia and Cristinel Ababei [13] have described algorithm is based on the balland-string model and employs a distributed approach based on partitioning of the regular NoC architecture into regions controlled by local monitoring units. Each local monitoring unit runs a shortest path computation procedure to identify the best routing path so that highly congested routers and faulty links are avoided while latency is improved. To dynamically react to continuously changing traffic conditions, the shortest path computation procedure is invoked periodically. Because this procedure is based on the ball-and-string model, the hardware overhead and computational times are minimal. Experimental results based on an actual Verilog implementation demonstrate that the proposed adaptive routing algorithm improves significantly the network throughput compared to traditional XY routing and DyXY adaptive algorithms. Ruizhe Wu et al. [14] have been described a new on-chip communication system & dubbed Wireless Network on- Chip (WNoC). This work centers on the design of a high-efficient, low-cost, deadlock-free routing scheme for domain-specific irregular mesh WNoCs. A distributed minimal table based routing scheme is designed to facilitate segmented XYrouting. Deadlock-free data transmission is achieved by implementing a new turn classes based buffer ordering scheme. Mohsen Nickray et al. [15] have described an adaptive routing algorithm which is based on deterministic XY routing algorithm. In their model a switch is a context-aware agent and a network is a society of context-aware agents which are ever learning and adapting to distribute the congestion uniformly and isolate the malformed switches (agents). In conventional XY routing, first, the load in the center of a network is much higher rather than total average and this leads to hot spot in the center of network. And second, a malfunction in switches could make part of network out of access. But in their proposed routing, first, all agents are aware from their neighbor's congestion and collaboratively try to route their input packets through less congested route, according to their experiences learned before and second, when a new malfunction takes place in the network, all agents collaborate each other to recognize the malformed agent and learn the best route. The main objective of their routing algorithm is to distribute network load uniformly throughout the network. They developed a NOC environment using SystemC. Masood Dehyadgari et al. [16] have described a pseudo adaptive routing which is an extension of classic XY routing. They consider mesh topology for evaluating proposed routing. Their switches use Pseudo adaptive XY routing algorithm. The load in the center of a network in ordinary XY routing is much higher rather than total average. This extra load on the center of mesh can cause spot hot. The main objective of their routing algorithm is to distribute network load. One of the advantages of distributing network load is balanced temperature on the mesh. Their routing algorithm has two modes that is deterministic and adaptive Packets are routed with classic XY routing (deterministic mode), when congestion in the network is low. When congestion is high, packets will be routed through less congested route adaptively (adaptive mode). Manas Kumar Puthal et al. [17] have described a new hierarchical cluster based adaptive routing called „C-Routing" in 2D mesh NoC. The solution reduces routing table size and provides deadlock freedom without use of virtual channels while ensuring livelock free routing. Routers in this method use intelligent routing to route information between the processing elements ensuring the correctness, deadlock freeness, and congestion handling. This method has been evaluated against other adaptive algorithms such as PROM, and Q-Routing etc. C-routing uses adaptively to avoid congestion by uniform distribution of traffic among the cores by sending flits over two different paths to the destination. Proposed technique achieves two objectives, as inferred from the results, reduction in area and higher throughput. These benefits are achieved at a marginal increase in power consumption and latency while preserving deadlock freedom with no extra virtual channels. Fault tolerance is another major issue in NoC design. Shu Yan Jiang et al. [18] describe an online detection method of interconnection for 2D torus structure of NoC system. This method can detect the data errors during transmission and identify the error results from the routing switch failure or the data transmission interconnection line failure. They design a sub-router based on

the wormhole exchange using E-cube routing algorithm and a check module which is suitable for the original routing node functions and work feature. They simulate the method by Verilog HDL and quartus II software. The experiment results show that the method can detect data errors caused by the router failure or interconnect failure and can locate the fault. Yang Quansheng & Wu Zhekai [19] have described an improved topology called Tmesh, which is based on standard mesh network by inserting four long links to connect the vertices to reduce the communication delay between some remote nodes. They also present a deadlock-free routing algorithm for Tmesh named TXY algorithm. The results of this algorithm show a certain reduction in the average packet delay and routing hops. When the network has 64 nodes, the average delay and routing hops of Tmesh are 2.92% and 3.53% lower than those of mesh respectively. A.H. Borhani et al. [20] described a new fault tolerant routing algorithm, which is based on dimension order routing, is proposed for k-ary 2-cubes. Packets are sent to their destination through XY routing algorithm and if this transmission is not possible, YX routing algorithm is applied. The result shows that these method is preferred, especially in the environments where the fault probability is low and the message generation rate is high. Xiaoqiang Yang et al. [21] described node coding and routing methods are important to the design of NoC. By the combination of network topology with corresponding, a two dimensional code based on Johnson code in Torus topology is proposed. The node coding implies the relation between neighboring nodes and has a good scalable characteristic. The two methods for code compressing are also presented to reduce the storage space of node address and increase the utilization rate of channel bandwidth. The improved algorithm for XY routing based on the code is presented and node structure is designed. The experimental results show combination of the code can simplify the routing algorithm in the implementation of NoC, decrease silicon resource consumption and greatly improve communication performance. Slavisa Jovanovic et al. [22] have been described a new deadlock free fault tolerant adaptive routing algorithm for 2D mesh NoC interconnection. The main contribution of this routing algorithm is that it allows both, routing of messages in the networks incorporating the regions not necessarily rectangular and routing to all nodes which are not completely blocked by faulty nodes. The proposed routing algorithm is based on a modified turn model and well known XY algorithm. The basic principle of this routing algorithm, prove its deadlock freeness, its feasibility and efficiency through the simulation results. Xiaohang Wang et al. [23] described a simple, yet efficient hardware based multicasting scheme is proposed for irregular mesh based NoC. First, an irregular oriented multicast strategy is proposed. Following this strategy, an irregular oriented multicast routing algorithm can be designed based on any regular mesh based multicast routing algorithm. One such algorithm, namely, Alternative XY (AL+XY), is proposed based on XY routing. Experimental results shows that AL+XY achieve significant reduction in power consumption and packet latency compared with existing solutions. AL+XY saves 29% power consumption than that of multiple unicast. In terms of average packet latency, when injection rate is high (e.g. near 0.15), the latency of AL+XY is only 50%. Mehrdad Seyrafi et al. [24] have been described a new fault tolerant routing algorithm with minimum hardware requirements and extremely high fault tolerance for 2D-mesh based NoCs is proposed. The LCFT (Low Cost Fault Tolerant) algorithm, removes the main limitations (forbidden turns) of the famous XY. So not only many new routes will be added to the list of selectable paths as well as deadlock freedom, but also it creates high level of fault tolerance. All these things are yielded only by the cost of adding one more virtual channel (for a total of two). Results show that LCFT algorithm can work well under almost bad conditions of faults in comparison with the Extended-XY, Extended-YX algorithms. Yonghui Li & HuaxiGu [25] described a new model called the XY-turn model for designing partially adaptive or deterministic routing algorithms for honeycomb networks on chip without adding virtual channels. The model prohibits two turns in opposite directions at some particular nodes so that the deadlock can be avoided. The restricted turns result in simplified router architectures especially for photonic NoCs. They have implemented a deterministic routing algorithm is carried out to test the performance of the algorithm in end to end delay and throughput under the conditions that messages length are 128 bytes, 256 bytes and 512 bytes respectively, as well as the network size varies from 36 cores to 64 cores and 98 cores. The results deterministic that the honeycomb NoCs would benefits from the XY-turn model in terms of communication efficiency.

III. MODELLING OF MESH TOPOLOGY

We consider some variants of 2D Mesh,2D Torus,3D Mesh topologies in this paper for study. In this topologies each switch is connected to four neighboring switches and one resource. The number of switches is equal to the number of resources. The resources and the switches are connected through communication channels. A channel consists of two unidirectional links between two switches or between a switch and a resource. We apply the deterministic XY routing algorithm for this topology. Mesh-based NoCs are receiving attention because of their modularity and the ability to expand by adding new nodes and links without any modification of the existing node structure. One advantage of a mesh is that it can be partitioned into smaller meshes, which is a desirable feature for parallel applications. Some of the most important performance parameters that are used in evaluating the NoCs, are defined in this section briefly. Latency over Network, presents the required time to transfer n bytes of payload from its source to its destination. Latency consists of routing delay, contention delay, channel occupancy and overhead. Bandwidth over communication is the amount of data that can be moved using a communication link in a unit time period. Throughput is the total number of received packets by the destinations per time unit. Packet Loss happens when one or more packets do not reach their destination due to the error

introduced by the network, the contention for network link or lack of buffer space etc. NS-2 is an open source, object-oriented and Tcl. Its a very common and widely used tool to simulate small and large area networks. Due to similarities between NoCs and networks, NS-2 has been a choice of many NoC researchers to simulate and observe the behavior of a NoC at a higher abstraction level of design. It has a huge variety of protocols and various topologies can be created with little effort. Moreover, customized protocols for NoCs can easily be incorporated into NS-2. The parameters for routers and links can easily be scaled down to reflect the real situation on a chip. Based on this fact, we have successfully simulated a 16x16 nodes 2D Mesh,2D Torus,3D Mesh based NoC using our reliable protocol for safe delivery of packets.

A.Simulation Environment

For the evaluation of event-driven simulator has been developed for the simulator models a 256 nodes 2D Mesh(16x16),2D Torus(16x16),3D Mesh (18x18) in which routing decision will be taken at input node using source routing methodology. Each node is connected with peer-to-peer twodirectional serial links. The connections are resource-router and router-router base having Transmission Control Protocol (TCP) with static routing table which established the path using shortest path algorithm. The Queue is drop tail type. The transport agent attached to source node N(0) is TCP and two different traffic pattern applications namely FTP and CBR were tested. FTP is use to transmit bulk data and CBR is use to generate packet at constant bit rate and transmit to destination node. Here four types of scenarios are modeled as descried in Table 1. These scenarios are revolving round the parameters by varying CBR or FTP, link delay and bandwidth, queue size and packets size. All these modeled parameters are described as a script file using Tcl. The parameters chosen for simulation are shown in table 1 under various scenarios. Here, node N(0) and node N(253) were fixed as source and destination node respectively for simulation.

Scenario-1:-Throughput and delay calculation with varying packet size

The link bandwidth and delay of link was kept constant at 10Mbps and 10ms, the bulk data size and constant data was generated using FTP and CBR (10Mbps) rate application with varying packet size generated. It is observed (Fig.1a) that for FTP and CBR application as the packet size increases throughput increases linearly initially and saturates for packet size in range of 6 to 512 Kbytes per second . The throughput for the 2D Torus is higher than 2D Mesh,3D Mesh topology which is due to higher length of path.

TABLE 1: VARIOUS SCENARIOS OF 4X4 AND 8X8 MESH TOPOLOGIES OVER FTP AND CBR TRAFFIC APPLICATIONS.

NoC Model Parameter		**Parameter Constraint applied in NS2**	
Topologies		2DMesh,2D Torus,3DMesh	
Connections		Resource-Router, Router-Router	
Transmission Protocols		Transmission Control Protocol(TCP)	
Routing Scheme		Static	
Routing Protocol		Shortest Path	
Queue Mechanism		Drop Tail (FIFO)	
Simulation time		20 seconds	
Number of Nodes		16x16(256 nodes)	
Scenario 1	**Scenario 2**	**Scenario 3**	**Scenario 4**
CBR :10Mbps; Link delay: 10ms; Link BW: 10Mbps Queue Size: 100; Varying packet size: 0.1 to 16000 Kbytes	CBR :10Mb/s; Link delay: 10ms; Link BW:10Mbps Queue Size: 5 to 200;Fixed packet size: 0.512 and 64 Kbytes	CBR :10Mb/s; Link delay:10ms; Link BW varying :10 to 200; Queue Size: 100; Fixed packet size: 0.512 and 64 Kbytes	CBR :10Mb/s; Link delay: 10-200ms; Link BW:10Mbps;Queue Size: 100; Fixed packet size: 0.512 and 64 Kbytes

Further, we also studied the performance of delay (Fig.1b) using FTP and CBR (10Mbps) rate application with varying packet size generated. It is observed (Fig.1a) that for FTP and CBR application as the packet size increases delay slowly increases and is highest from the 1000 to 10,000 packet size and later drop down drastically. The delay for the 2D Mesh,3D Mesh is higher than the 2D Torus topology which is due to higher path length.

Scenario-2:-Throughput and delay calculation with varying queue size with low and high load packets

In this scenario we kept each link bandwidth at 10Mbps, propagation delay of the each link at 10ms, the bulk data size and constant data was generated using FTP and CBR (10Mbps) rate application with varying queue size from 5 to 200. It is observed (Fig.2a) that the performance of low load i.e. 0.512Kbytes is very low as compared to high load of 64 Kbytes having factor of 4-5 times. This is because at low load of 0.512Kbytes the network resource i.e. queues size is not utilized efficiently. Also it may be noted that the within the low load, the 2D Torus has higher throughput as compared to 2D Mesh,3D Mesh topologies due to short path length. This holds same for high load packets wherein the 2D Torus topology has higher delay throughput as compared to 2D Mesh,3D Mesh topology due to short path length.

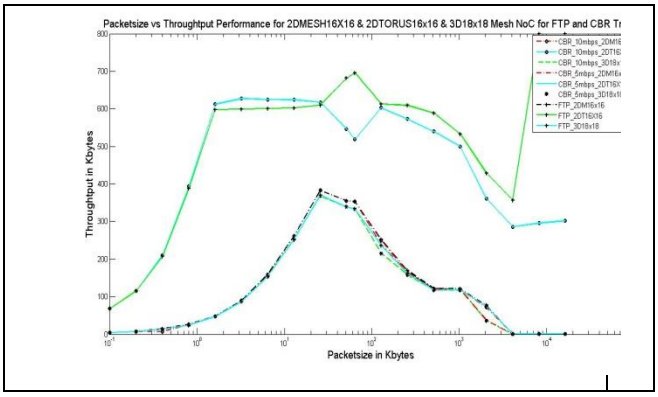

Fig. 1. (a) Throughput v/s Packet size for 2D Mesh(16x16),2D Torus(16x16),3D Mesh (18x18) topology for CBR and FTP application.

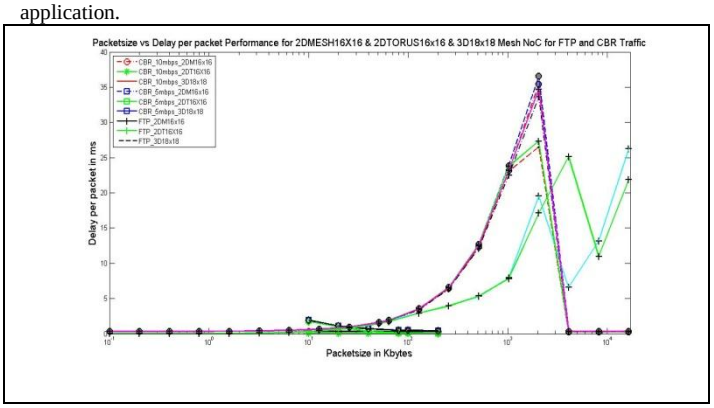

Fig. 1. (b) Delay per packet v/s Packet size for 2D Mesh(16x16),2D Torus(16x16),3D Mesh (18x18) topology for CBR and FTP application.

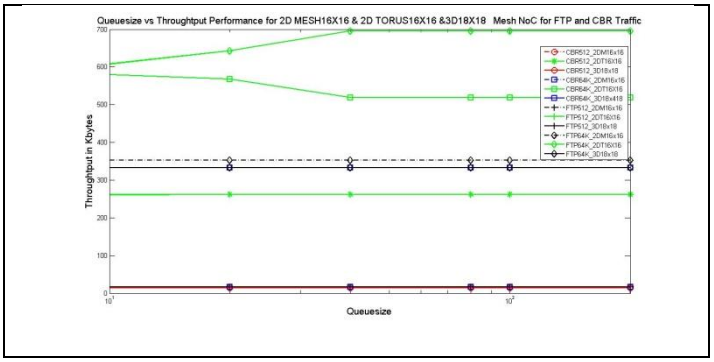

Fig. 2. (a) Throughput v/s Queue size

Similar performance was studied for transmission delay from N(0) to N(15) and N(0) to N(64), N(0) to N(256) source and destination node respectively. It is observed (Fig.2b) that the delay performance of low load i.e. 0.512Kbytes is very low as compared to high load of 64 Kbytes having factor of 4-5 times on an average. This is because at low load of 0.512Kbytes the network resource i.e. queues size is not utilized efficiently. Further it may be noted that within the low load, the 2D Torus topology has better performance over transmission delay as compared to 2D Mesh,3D Mesh topology. It may be noted that the delay performance over higher load is saturating at the queue size of 40. Better performance for transmission delay over 2D Torus topology as compared to 2D Mesh,3D Mesh topology, which is due to higher path length.

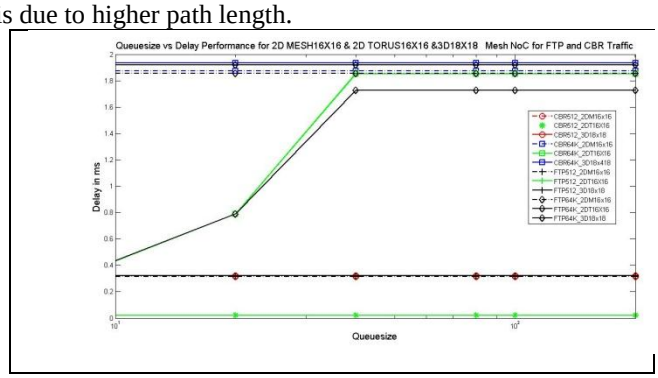

Fig. 2. (b) Delay per packet v/s Queue size

Scenario-3:- Throughput and delay calculation with varying link Bandwidth for low & high load packets

In this scenario we kept queue size as 100, propagation delay of the each link at 10ms, the bulk data size and constant data was generated using FTP and CBR (10Mbps) rate application with varying link bandwidth from 10 to 200. It is observed (Fig.3a) that the throughput performance for low load i.e. 0.512Kbytes is very low below 100 Kbytes compared to high load of 64 Kbytes having average factor of 20-25 times. This is because at low load of 0.512Kbytes the bandwidth is not exploited and so throughput remains very low. At the high load of 64Kbytes FTP performs better as compared to CBR, as CBR rate is low to exploit the given bandwidth and hence it remains saturated even after increasing bandwidth. While the FTP application the bandwidth is linearly increasing as the bandwidth increases and it is found to be best for 2D Torus topology as compared to 2D Mesh,3D Mesh topology due to path length.

Similar performance was studied for transmission delay from N(0) to N(15) and N(0) to N(64), N(0) to N(256) source and destination node respectively. It is observed (Fig.3b) that the delay performance of low load i.e. 0.512Kbytes is better as compared to high load of 64 Kbytes having factored of 4-5 times on an average between bandwidth of 10-40 Mbps. The initial delay is high for the low link bandwidth within 10-40 Mbps as for the higher load the bandwidth is not enough for transmission.

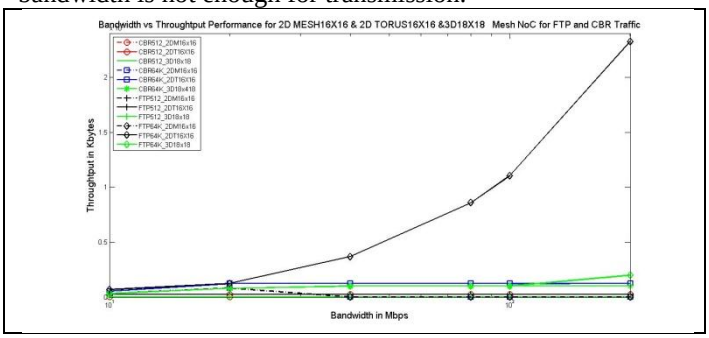

Fig. 3. (a) Throughput v/s Bandwidth

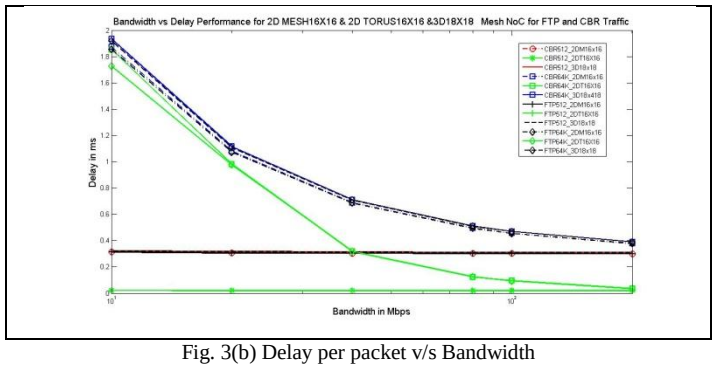

Fig. 3(b) Delay per packet v/s Bandwidth

Scenario-4:-Throughput and delay calculation with varying propagation delay of link with low & high load packets

In this scenario we kept queue size as 100, link bandwidth from 10Mbps and the bulk data size and constant data was generated using FTP and CBR (10Mbps) rate application with varying link propagation delay each link within 10-200ms. It is observed (Fig.4a) that the throughput performance for low load i.e. 0.512Kbytes is very low below 100 Kbytes compared to high load of 64 Kbytes factor of 4-5 times, having average value of having average of 400 Kbytes. The throughput of the high load decreases as the link propagation delay increases. The 2D Torus topology performs better compared to 2D Mesh,3D Mesh due to low path length. The decrease in performance at the higher propagation delay is natural and implicit.

Similar performance was studied for transmission delay from N(0) to N(15) and N(0) to N(64) , and N(0) to N(256) source and destination node respectively. It is observed (Fig.4b) that the delay performance is better over topologies as compared to scenarios 2 and 3 which was for high and low loads. The transmission delay remains within average value of 1.5ms for high load packets i.e. 64Kbyts; using FTP and CBR (10Mbps) rate application. This could be because as the propagation delay increases the packets transvers time matches with that of propagation delay and system is seems to be in unison within specific propagation link days limits. While in other application low load 2D Mesh,3D Mesh topology and 2D Torus load topology the packets delay performance degrades.

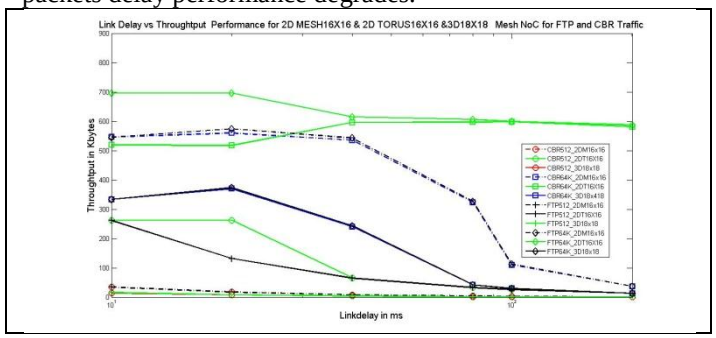

Fig.4. (a) Throughput v/s Link delay

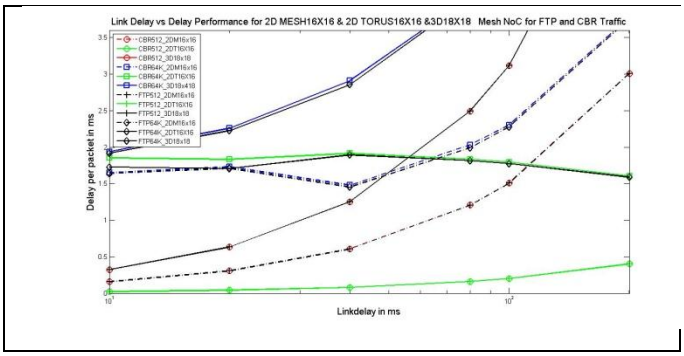

Fig. 4. (b) Delay per packet v/s Link delay.

IV. DISCUSSION AND CONCLUSION

Choosing suitable parameter for NoC architectures is an important issue in NoC design and implementation so as to bringing the NoC paradigm to real applications. Here, we have presented and developed simulation and verification platform to measure the NoC performance in terms of network delay and throughput. The proposed platform has been designed and implemented in 2D Mesh(16x16),2D Torus(16x16),3D Mesh (18x18) topology. Here we have proposed a NoC platform to meet the requirements of the target applications by customizing parameters. The designers can configure various heterogeneous and homogenous network topologies, flow control mechanisms and routing algorithms as well as configure a various regular applications. Here we have evaluated the performance of standard 2D Mesh(16x16),2D Torus(16x16),3D Mesh (18x18) NoC architecture. Each node is connected with point-to-point bidirectional serial links. Our work briefly compares the performance of the NoC, for the throughput and delay. Using different attributes, like varying packet size; FTP traffic gives better performance as compared to CBR traffic. The varying packet size has little effect on throughput performance in FTP but significance effect in CBR up to packet size of 25Kbytes. With respect to delay CBR traffic performance is better than FTP traffic, as packet size increases, the delay increases in FTP but there is not much change in delay in CBR traffic. Varying Queue size with high load packets, FTP traffic gives better performance as compared to CBR traffic, throughput increases with increase in queue size in FTP. Delay increases as queue size increases in FTP and CBR traffic. Link Bandwidth for low load and high load, is total with varying link bandwidth for low and high load FTP traffic, which gives better throughput as compared to CBR traffic and delay decreases as bandwidth increases in both the traffic. Propagation delay of link with low load and high load, Throughput decreases as propagation delay of link increases for FTP traffic with low and high load. Better in FTP traffic, delay per packet increases as propagation delay of link increases in both the cases. The extension of these work is to evaluate the lowest drop probability using different CLICH, BFT algorithm, then will be find the good topology of the system.

Hence the simulations, considerable end-to-end throughput enhancement, and a reduction in average delay was measured

when using 2D Mesh(16x16),2D Torus(16x16),3D Mesh (18x18) topologies. Using such a technologies appropriately, higher service support can be provided to clients with increased throughput while meeting more efficiently QoS requirements demanded by today's applications. Finally a simple sensible situation was exhibited which highlighted how 2D Mesh(16x16),2D Torus(16x16),3D Mesh (18x18) work topologies help in the versatility of WMNs. It was highlighted that when WMNs are gently stacked, the future extent of MIMO STBC modes can be used to boost scope utilizing a negligible number of 2D Mesh(16x16),2D Torus(16x16),3D Mesh (18x18) work switches.

XY routing algorithm is one of the simplest and most commonly used NoC routing algorithms. It is deterministic, static and deadlock free routing algorithm. We observed that most of the XY routing algorithms are implemented on 2D mesh,3D mesh topology to increase throughput & reduce latency. But most of them is facing problem of traffic congestion in the centre. There are number of topologies available but the torus topology has gained lots of consideration by designer due to their simplicity. So we propose new design method using a XY routing algorithm for 2D torus topology to solve above problem. We expect the result with reduce the average latency per packet and increase average throughput.

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