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Sensor's data transmission with BPSK using LDPC (Min-Sum) error corrections over MIMO channel: Analysis over RMSE and BER

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ABSTRACT

Low-Density Parity Check (LDPC) code meets the desired performance for extended code lengths and binary fields. LDPC codes offer noteworthy error correction performance and also increase the design overhead for wireless communication systems. LDPC codes can offer proximity to Shannon Limit performance, when execution complexity and latency are not system boundaries, by using large code lengths and ever-increasing the number of iterations in the decoding process. Here in this paper, we have demonstrated data reduction method using Principal Component Analysis (PCA) for fuse data at sensor level to transmit and regress the same at the receiver for improvising the channel capacity of the system. We have fused 45 signals sensor data having a bandwidth from 50 Hz to 2500 Hz, sampled at 5 KHz each. The regression is measured using the RMSE between the transmitted and received signals. Also, the communication system has demonstrated the BER performance of the 2-Phase shift keying (BPSK) modulation technique with and without LDPC decoder (Min-Sum) for 2×2, 3×3, 4×4 Multiple Input Multiple Output (MIMO) channel. The performance parameters for data regression and data communication error is evaluated over AWGN channel ranging from −15 dB to 40 dB SNR. The proposed system is useful for the next generation low bandwidth communication system such as wireless systems developments, i.e., WiMAX and 4G, 5G, 6G.

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1. Introduction

Low-Density Parity-Check (LDPC) codes are recognized as they are the most powerful forward error correction codes, whose bit-error-rate (BER) performance is very near to the Shannon limit. LDPC codes are proved to have better performance and quite a lot of advantages over other error correction codes such as Hamming codes, Turbo codes, Reed-Solomon and Reed-Muller codes. LDPC codes are broadly used in many applications such as Terrestrial television broadcasting system, digital satellite, and Digital Video Broadcasting. Though the decoding algorithm in LDPC is modest, as we go on increasing the block length LDPC matrix becomes larger, and it is time-consuming to connect and test the connections physically. In this paper, an automated high-level design approach is discussed. The communication system is demonstrated for the fusion of data at the sensor level for 45 signals spread over the bandwidth of 50 Hz–2500 Hz. These signals are fused using the well-known data reduction method, i.e. Principal Component Analysis (PCA) and regressed at the receiver level to generate the original signals. This system is demonstrated for the BPSK modulation over the LDPC error correction Min-Sum algorithm for the Multiple Input Multiple Output (MIMO) system. The evaluation of this system is performed over Signal to Noise ratio of −15 dB to +40 dB for RMSE and BER performance. We are using MATLAB Simulink (2018B) for modeling the said system. The paper organized as follows. Section 2 presents the previous work done in the Min-Sum algorithm. Section 3 explains the theory of the Min-Sum Algorithm. Design methodology for developing the LDPC decoder in MATLAB Simulink given in Section 4. Simulation results are covered in Sections 5 and 6 concludes the paper.

1.1. Motivation

The main goal in designing a communication system is to achieve reliable data transmission for the power efficiency having

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the lowest error probability (bit error rate). Moreover, a higher data rate with a constraint on available bandwidth is another target. LDPC codes can be selected as an excellent coding scheme to achieve the highest reliability transmission in noisy channels. On the other hand, in terms of efficient use of bandwidth while having a high data rate to achieve good channel capacity should be explored. Therefore, motivated by the development of low power and enhance channel capacity over low bandwidth for various SNR is a challenge. We tried to address this problem using sensor level, data reduction method over MIMO system to improvise the channel capacity by some factor in a wireless communication system.

1.2. Paper contributions

This paper is devoted to the study of sensor level fusion of data transmission over BPSK modulation using LDPC Min-Sum Error Corrections over MIMO Channel. The appear contributions are the following:

- Present the sensor level data fusion of signals originating from 45 sources for efficient transmission and reception over the communication channel for performance parameters like RMSE.
- The same system analyzed and evaluated over LDPC decoder algorithm for error-free data transmission with noisy channel using BPSK Modulation for performance parameters like BER.
- The System is further analyzed for the wireless communication system for data transmission with and without 2×2, 3×3, 4×4 MIMO channel respectively in AWGN channel.

2. Previous work

LDPC decoder uses various message passing algorithm for decoding information. The Min-Sum algorithm is one among the LDPC algorithm. The bits to be sent are generated as $k \times G$, where the message of k-bits gets multiplied by G-matrix also called a generator matrix. LDPC codes have a code rate which is represented by k/n. Here k is the number of original bits in the message and n is the total encoded information.

These encoded n bits are directed by a transmitter, over an AWGN channel, then at receiving end decoder decodes the n-bits using message passing algorithm to obtain original k bits. The LDPC codes are usually represented by Tanner Graphs.

LDPC codes can be denoted by matrix, typically called H-matrix. The H matrix generally contains zeros and a sparse density number of 1's [1,2] and hence the title low name density. It is also represented by a graph called tanner or bipartite graph. Because of exceptional BER, LDPC codes are comprehensively used in standards such as 10 Gigabit Ethernet, Wi-MAX, Digital video broadcasting (DVB-S2) and anticipated to be part of many forthcoming standards [3].

The Min-Sum algorithm (MSA) [4] is the modified version of the Sum-Product algorithm (SPA) [4]. The Min-Sum algorithm has a simplified operation which reduces the complexity of the algorithm. The check node operation is simplified [4]. The Min-Sum algorithm helps design of semi-parallel architecture this saves the hardware resources while implementing on target hardware like FPGA [5]. The advantage of fully parallel architecture gives high throughput and it does not need memory to store results. Thus, fully parallel architecture is also power efficient. But partially parallel architectures have comparatively lower throughput. However, the decoding circuit is much smaller and area efficient [5]. Error correction algorithms are often realized in hardware for fast processing to meet the real-time needs of communication systems. Though, traditional hardware implementation of LDPC decoders needs large amount of resources. Due to the complex interconnections among the variable and check nodes of LDPC decoders, it is very time-consuming to use earliest hardware description language (HDL) based approach to design LDPC decoders [6]. So it is possible to use assisting tools in this development. To test and validate the design simple MATLAB application can be used for higher block length [7]. It is very difficult to simulate and test the whole design in HDL especially when the block length of the design becomes large and simulation computation time is sufficiently large. Due to this, for validation purpose, the complete design will be implemented in MATLAB [8]. As shown in Fig. 1 the simulation of the LDPC decoder is done in MATLAB Simulink using MATLAB (2018B).

3. Min-Sum algorithm of LDPC

The algorithm encodes an input binary message k to n-bit codeword. At the decoder side min-sum algorithm is used as message passing algorithm. Decoder performs iterations for parity check and Check node (CN) and Variable node (VN) are updated as shown in step2 and step3. Here, LLR's (Log Likelihood Ratio) are exchanged as messages between CN and VN. The LLR of VN is performed by step 4. The options for decision type available in this algorithm are hard and soft decisions. When you set this parameter to hard decision, the output is decoded bits.

Let C be a regular LDPC code of length N and dimension K whose parity-check matrix *A* with M = N-K rows and N columns contains exactly d_v 1's in each column (column weight) and exactly d_c 1's in each row (row weight) A_{mn} is the value of the m_{th} row and n_{th} column in *A*. The set of bits that participate in check is denoted:

$N_m = \{n{:}A_{mn=1}\}$. The set of checks that participate in bits $M_n = \{m{:}A_{mn=1}\}$.

Assume codeword, $C = [C_1, C_2, C_3, \ldots\ldots C_N]^T$ Before transmission, it is mapped to a signal constellation to obtain the vector, $t = [t_1, t_2, \ldots t_N]^T$

where

$$t_n = 2 * C_n - 1$$

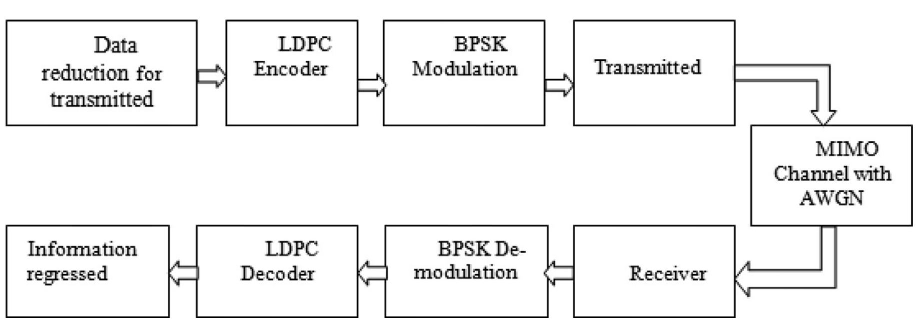

Fig. 1. The proposed Sensor's Data Transmission over BPSK Using LDPC Error Corrections Over MIMO Channel.

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which is transmitted through an AWGN channel with variance $\sigma^2 = N_0/2$

$$r = [r_1, r_2, r_3, \ldots\ldots r_N]^T$$

where

$$r_n = t_n + v_n.$$

here, is the Additive White Gaussian Noise (AWGN) with zero means. Let hard decision vector,

$$z = [\, z_1, z_2, z_3, \ldots\ldots z_N]^T$$

$$z_n = \mathrm{sgn}(r_n)$$

Where $\mathrm{sgn}\ (r_n) = \begin{cases} 1, & r_n \\ 0, & Otherwise \end{cases}$

L_n: A priori information of bit node, n.

$\overline{L_n}$: A posteriori information of bit node, n.

$E_{m,n}$: The check to bit message from m to n.

$F_{n,m}$: AThe bit to check message from n to m.

Step 1: Initialization

A priori information, $L_n = -r_n$

Bit to check message initialization, $F_{n,m} = L_n$

Step 2: Horizontal Step

Check node Processing:

$$E_{m,n} = \log\frac{1 + \Pi_{n'\varepsilon N(m)\ n}\tanh(F_{n'.m}/2)}{1 - \Pi_{n'\varepsilon N(m)\ n}\tanh(F_{n'.m}/2)} \tag{1}$$

Step 3: Vertical Step

A posteriori information:

$$\bar{L_n} = L_n + \sum_{m\varepsilon M(n)} E_{m,n}$$

Bit node Processing:

$$F_{m,n} = \bar{L_n} + \sum_{m'\varepsilon M(n)} E_{m,n}$$

Step 4: Decoding Attempt

$\overline{L_n} > 0, \overline{c_n} > 0,\ \ else\overline{c_n} = 0$

If $A\overline{c_n} = 0$ then the algorithm stops and $\overline{c_n}$ is considered as a valid decoding result.

Otherwise, it goes to next iteration until the number of iteration reaches its maximum limit [9].

Min-Sum algorithm is the modified form of the sum-product algorithm that reduces the implementation complexity of the decoder.

This can be done by altering the Horizontal step:

$$E_{m,n} = \log\frac{1 + \Pi_{n'\varepsilon N(m)\ n}\tanh(F_{n'.m}/2)}{1 - \Pi_{n'\varepsilon N(m)}\tanh(F_{n'.m}/2)}$$

Using the relationship:

$$2\tanh^{-1}p = log\frac{1+p}{1-p}$$

Equation (1) can be rewritten as,

$$E_{m,n} = 2\tanh^{-1}\prod_{n/\varepsilon N(m)}\tanh(f_{m,n}/2)$$

$$E_{m,n} = 2\tanh^{-1}\prod_{n/\varepsilon N(m)}\mathrm{sgn}(f_{m,n}/2)\prod_{n/\varepsilon N(m)}\tanh\left(\frac{f_{m,n}}{2}\right) \tag{2}$$

The Min-sum algorithm simplifies the calculation of (2) even further by recognizing that the term corresponding to the smallest $F_{n,m}$ dominates the product term and so the product can be approximated by a minimum:

$$E_{m,n} = \prod_{n/\varepsilon N(m)}\mathrm{sgn}(f_{m,n}/2)$$

Table 1
Variables are using proposed system.

Parameters	Value
LDPC code rate	½(32,400/64,800)
LDPC Encoder Input Type	Bit
LDPC Decoder output Type	Information Part
LDPC Decoder Decision Input Type	Hard Decision
LDPC Decoder Number Of Iterations	50
Modulator Type	BPSK
Modulator Input Type	Bit
Modulator Symbol Order	Binary
Demodulator Output Type	Bit
LLR Algorithm	LLR
Channels	SISO&2 × 2, 3 × 3, 4 × 4 MIMO
Channel Noise Factor	SNR

In this MIN-SUM algorithm first we initialize the bit to check message. Then update the check message in the horizontal step. In this step, multiply the Optimization factor with the check message. After that, proceed to the vertical step. In this step, we update the posterior information with the help of check message and then we update the bit node. Here, multiply the Optimization factor with the check message. The last step is the decision making process. If the decoded codeword is correct, we stop there and take it as the output or otherwise repeat the whole decoding process until the iteration number reaches its maximum limit [9,11].

4. Design methodology

Efficient implementation of higher Block length LDPC decoder is a time-consuming process hence to overcome, we have designed LDPC encoder and decoder in MATLAB Simulink (2018B). Using Simulink library in communication system, we have provided streams of data in matrix form of block length (100, 45) of 16-bit wordlength corresponding to 45 sensors signal data. This is reduced to (45, 45) of 16-bit wordlength Eigen matrix corresponding to 45 sensors signal data. This reduces matrix is mapped to LDPC for the code rate of R = 1/2 to generate the block length of 64,800 bits at he LDPC encoder having 32,400 message bits. The encoded data from LDPC encoder is further BPSK modulator with 2 bits per symbol. Channel selected here is AWGN having SNR values from −15 dB to 40 dB. The said system is further tested for the performance over LDPC codes with 2 × 2, 3 × 3, 4 × 4 MIMO for wireless communication application Table 1.

5. Results analysis

We use a class of irregular pseudo-random LDPC codes which were proposed by Neal [10] to simulate the error performance over an AWGN channel. The block length (32,400, 64,800), having code rate R = 1/2, the average column weight Wc = 4 or 8 and the average row weight Wr = 8 or 12. The maximum number of iterations decoders are set 50, respectively.

We have presented the RMSE performance in Fig. 2. The performance is for BPSK modulation with and without LDPC error correction over AWGN channel having SNR −15 dB to +40 dB. One can see that the performance of RMSE is better with LDPC algorithm as compared to the without LDPC error corrections for 1 × 1, 2 × 2, 3 × 3 and 4 × 4 MIMO channel. The RMSE is 0.4e−4 (0.4×10^{-4}) for 1 × 1 LDPC MIMO at −03 dB SNR value. The RMSE is 0.4e−4 (0.4×10^{-4}) for 4 × 4 LDPC MIMO at −10 dB SNR value. This state that one can have error-free signals transmission up to −10 dB with LDPC error correction coding.

We have also presented the BER performance in Fig. 3. The performance is for BPSK modulation with and without LDPC error correction over AWGN channel having SNR −15 dB to 40 dB. One can see

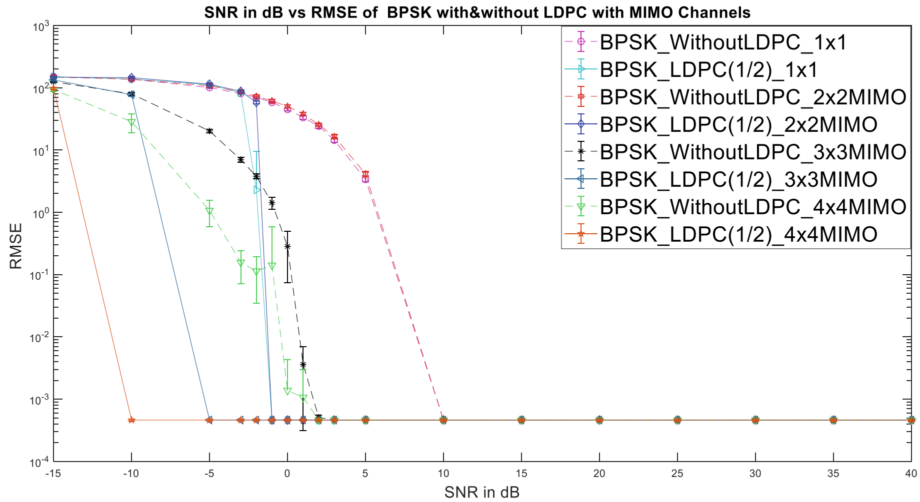

Fig. 2. RMSE performance of LDPC code with code rate R = 1/2 over an AWGN channel via BPSK modulation.

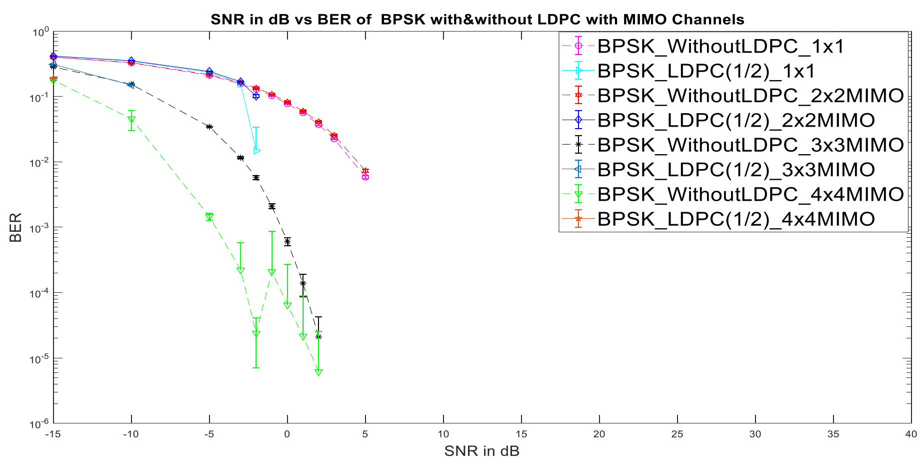

Fig. 3. BER performance of LDPC code with code rate R = 1/2 over an AWGN channel via BPSK modulation.

that the performance of BER is better with LDPC algorithm as compared to the without LDPC error corrections for 1×1, 2×2, 3×3 and 4×4 MIMO channel. The BER value at the e$-2(10^{-2})$ is -7.5 dB, -3dB, 4 dB and 5 dB respectively for 4×4, 3×3, 2×2, and 1×1 MIMO without LDPC. This implies that 4×4 is performing better compared to 1x1 MIMO for error correction. The BER value at the 0.1e-1 (0.1×10^{-2}) is -15 dB, -10 dB, -3dB and -2dB respectively for 4×4, 3×3, 2×2, and 1×1 MIMO with LDPC. This implies that 4x4 is performing better with LDPC compared to without LDPC.

Vinaya et al. [11] specified that the results of BER performance improve with an increase in block length which can be optimized for error correction by setting the number of decoding iterations between 5 and 50 for SNR close to 2 dB. Since, more errors are introduced for larger frame lengths and hence the number of iterations needs to be increased for better Error Correction performance.

6. Conclusion

Similar works are found like Raghuwansi et al., here the BER achieved is 10e-6, varying with the changes in modulation techniques as well as FFT points, which says that with 256 FFT points BPSK modulation the wireless LDPC based MIMO-OFDM system outperform[12]. Indira Bestari et al., presented LDPC encoding process which gives BER value of 10e-7 at SNR -6.0 dB. Here, LDPC encoding works very well on a single RF-based MIMO OFDM system even on the negative value of SNR dB. The coding rate also needs to be noted which states that the smallest rate will require a larger parity matrix so as to produce a higher level of accuracy in the error correction process. The process of channel estimation also works very well by generating a very small difference between theoretical and estimation values[13].

Madiop et al., investigated about the complexity and BER performance analysis of Maximum likelihood zero forcing and minimum mean square error MIMO receivers by using a small length binary polar code. The performance gain of 3 dB at 10e-2 of the proposed is obtained compared to the optimal maximum likelihood detector. Zero Force is always the worst performance as in the literature[14]. Lamia et al., demonstrate that the channel codes provide high channel efficiency with small code rate, low decoding complexity and low BER. They demonstrated the concatenated BCH-CC-LDPC for MIMO system. Also, the concatenated scheme improves the performance of a low receive diversity MIMO system. Finally, the concatenated schema enhances the system decoding latency because an LDPC decoder is replaced by a CC decoder and a short BCH decoder, which have lower decoding latencies than LDPC. The performance of the proposed system could also be enhanced in case of LDPC convolutional codes [15]. Touhidul Islam et al., presented BER performance of the 1/2-rated LDPC channel encoded STTC MIMO-OFDM system under different digital modulations on a Raleigh fading channel,

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which degrades due to fading channel effect. The system outperforms at BPSK modulation and shows worst performance at QPSK modulation; the system with QPSK modulation is more influenced by the Doppler frequency shift and its performance degrades. At Eb/N0 value of 0.75 dB, the system performance is improved by 2.7195 dB in the case of BPSK modulation as compared with QPSK [16].

Risto et al., proposed the soft decision decoding and signal combining algorithms of MRC and the Alamouti code to the orthogonal MIMO codes for three and four T_x antennas. The complexities of the novel combiners do not essentially exceed that of the Alamouti combiner, making them very attractive in terms of implementation. With the soft decision MIMO combiners, the FEC decoders attain the same error rates with 2–3 dB smaller data bit energy than with the hard decision MIMO. The novel combiners require a close to constant channel over four instants, implying that they are better suited for low mobility environments. The soft decision MIMO combiners provide the largest gain when linked to a bitwise soft decision demodulator. Extracting the bitwise LLR values from the combiner output symbols was shown to be a very simple task not only in QPSK but also in Gray-mapped 16-QAM. It is notable, however, that in order to get correct noise variance to the bitwise LLR equations, multiplication by the pertaining channel tap energies has to be carried out [17].

Ankita et al., shows low density parity check codes and space time block codes on far-end image reconstruction offers significant visual quality improvement at reduced data transmission. The proposed soft decision decoding scheme offers a coding gain of 3 dB at −2 dB channel signal-to-noise ratio for an 8 antenna system. Simulations show a coding gain increases with the increase in signal-to-noise ratio and the number of transmit antennas. Decoding performances of the block codes with zero and no-zero entries highlight the fact that the former offers marginally better bit error rate performance (around 0.5 dB for number of antennas less than 8) compared to the latter one, though zero entry codes give rise to peak-to-average power ratio problem [18]. Ibrahim et al., the BER performance of LDPC codes in Weibull fading channels were analyzed for different decoding rules by means of comparative computer simulations. An LDPC coded BPSK communication system was designed as a communication infrastructure to perform the analysis. Four different decoding rules and a regular LDPC code with (1008, 504) block length and ½ code rate were used in simulations [19].

In this paper, a brief overview of Min-Sum algorithm based LDPC decoder is presented. Among various message passing algorithms, one of the vital algorithms is Min-Sum which provides suitability for implementation of Decoder with less hardware implementation area. Also the Bit Error Rate calculated for BPSK is from 10e−1 to 10e−6 for SNR −15 to 5 dB. The data reduction methodology for enhancing the channel capacity of the channel has helped in designing high performance communication system specially in the low bandwidth wireless networks. For future work, we address the study of different Modulation techniques and their performance in terms of BER and RMSE efficiency versus SNR of received data.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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