FPGA BASED CONTROLLER DESIGN FOR SWITCHING CONVERTERS AND PERFORMANCE ANALYSIS

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By

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Dedication

This dissertation is dedicated to my husband, Dattatraya, who has been a source of strength, support and motivation throughout this research. I am truly blessed for having you in my life.

I also dedicate this dissertation to my dear parents and parents-in-law for their unconditional love, support and encouragement.

Thesis Approval

This thesis entitled **"FPGA BASED CONTROLLER DESIGN FOR SWITCHING CONVERTERS AND PERFORMANCE ANALYSIS"** by Smt. Sonali Dattatraya Pandit is approved for the degree of **Doctor of Philosophy in Electrical and Electronics Engineering.**

Examiners:

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Supervisor:

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Principal:

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Date:

Place:

DECLARATION

I, Sonali Dattatraya Pandit, hereby declare that this thesis represents work which has been carried out by me and that it has not been submitted, either in part or full, to any other University or Institution for the award of any research degree.

Place: Farmagudi, Ponda — Sonali Dattatraya Pandit

Date:

CERTIFICATE

I hereby certify that the work was carried out under my supervision and may be placed for evaluation.

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SONALI PANDIT

Abstract

Electronic devices like cell phones, laptops require multiple dc supplies for charging and connecting various components like LCD display, USB devices. The AC-DC and DC-DC converters find a variety of applications in modern gadgets. They are also used in motor drives and power control. These switch mode converters employ a controller in the feedback loop to regulate the dc output voltage. A variety of controllers, both analog and digital, are used with different control techniques. The controllers designed are of various technologies like analog, microcontroller, neural network, fuzzy logic, DSP and VLSI etc. VLSI system design has the better advantages of high speed, small area, low cost, reliability and reprogrammability. In this research, design and implementation of a controller for switching converters using the FPGA based design and VLSI technology is proposed. Buck and boost converters were designed and analyzed using the state space averaging method. Simulations were performed using Matlab Simulink for an open loop and closed loop control. Different types of compensators viz, PI, Lead, Lead with PI and PID were designed and simulated in Simulink environment for these converters. Comparison of all these proposed compensators in time and frequency domain is analyzed. Compared to the uncompensated converter, PI controller so designed improves the phase margin from 19.1° to 27.4°. The gain cross over frequency is also increased to 1.31 krad/s from 960 rad/s. Using a PID controller, the phase margin obtained is 49.2°, its overshoot is 0.03% and a settling time of 1.5 msec.

PI and PID controllers were designed using the platform of VHDL language. Finite state machine modeling is adapted to implement the said controllers. The control loop consisting of a digital comparator, digital controller and the pulse width modulator is implemented on Spartan 3M FPGA. An onboard analog to digital converter (ADC) is interfaced using VHDL. Xilinx 14.1 Project Navigator is used to simulate and synthesize the control loop. Functional simulation is performed using ISim simulator. Logic analyser Chipscope, which is implemented in the FPGA is used to obtain the PWM output in real time. The buck and boost converters were implemented on hardware and interfaced with the proposed PI and PID controllers. Performance of the converters is tested with open loop and closed loop configurations for varying input voltage and varying load currents. An optimum controller is proposed using the design aspects of finite state modeling. Voltage regulation is improved using a PI and a PID controller. The finite state machine modeling of a PID controller has a reduced hardware of 112 slice flipflops and 60 LUT's as compared to a multiplier based

controller.

The switching devices in the converter and the associated passive components in the switching converters will give rise to non-linearity. The buck and boost converters are analyzed for the non linearity. The discrete iterative maps for the converters were derived. The discrete maps were simulated in Matlab environment for variations in input voltage and reference current to obtain the bifurcation diagrams. The output of the converters is obtained for the input voltage in the period 1, period 2 and chaos regions using Matlab Simulink. Non linearity regions of the converters were observed wherein the switching converters exhibit chaotic behavior of operation.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

The demand and usage of modern electronic devices like cell phone, laptops, portable chargers and portable DVD players, solar cells etc. are increasing. These devices and their components need constant operating voltages and current. This is achieved by converters. AC-DC or DC-DC converters supply the necessary voltages by either stepping up or stepping down the levels. The constant output in the devices is taken care by a controller in the feedback path. DC-DC converters require to convert a fixed dc source into a variable dc source by either stepping up or stepping down the voltage. Switched-mode converters are DC-DC converters that supply dc loads with a regulated output voltage, and protection against over currents and short circuits.

The advantages of switched mode converters are

1. High Power Conversion efficiency.
2. Small size of passive components since they operate at high switching frequencies.
3. Reduced thermal losses.

DC-DC power converters find their use for personal computers, office equipment, spacecraft power systems, laptop computers, telecommunications equipment and dc motor drives and control circuits.

1.1 Types of DC-DC converters

A switching converter is an electronic circuit that converts power using switching devices that are turned on and off at high frequencies, and storage components such as inductor or capacitor to supply power when the switching device is in its non-conduction state.

DC-DC converters can be classified into two different types [1]- [5]

- **DC-DC converters without isolation**

  These DC-DC converters do not have any isolation transformer between input and output stages. Some of the commonly used DC to DC converters without isolation are

  a. Buck converter

  b. Boost converter

  c. Buck-boost converter

  The buck converter is step down converter (input voltage greater than the output voltage) whereas boost converter is a step up converter (input voltage less than the output voltage). The buck boost converter is derived from step up and step down converters. The buck boost converter can be operated in step up or step down mode based on duty cycle of switch. The step down and step up converters are basic converter topologies based on which other converters are derived.

- **DC-DC converters with isolation**

  In this type of converter, a transformer is provided in between to isolate the input and output stages. The electrical isolation is an additional feature and is mainly useful in cases where the input voltage level (Vin) and output voltage level (Vout) differs significantly i.e. high or low values of Vout/Vin. The DC-DC converters with isolation is again divided into two types based on polarity of transformer core excitation

  a) Unidirectional core excitation where core is excited with forward currents of only one direction. In these converters the isolation transformer core is operated in only the positive part of B-H curve.Some of the commonly used DC-DC converters with unidirectional core excitation are

  a. Fly back converter (derived from buck-boost converter)

  b. Forward converter (derived from buck converter)

  c. Full-bridge converter (derived from buck converter)

  d. Half-bridge converter (derived from buck converter)

  e. Push-pull converter (derived from buck converter)

  b) Bidirectional core excitation where core is excited with currents in either direction. In these converters the isolation transformer core is operated alternatively in positive and negative portions of B-H curve. Some of the commonly used DC-DC converters

with bidirectional core excitation are

a. Flyback and forward converters.

b. Push-pull, half-bridge and full-bridge converters.

c. Resonant DC-DC converters.

Figure 1.1 shows the basic types of converters used in switched mode supply. The cuk converter is a buck boost converter with a low ripple current. Single-ended primary-inductor converter (SEPIC) is a type of DC-DC converter that allows the output voltage to be greater than, less than, or equal to that at its input. Zeta converter is a fourth-order DC-DC converter made up of two inductors and two capacitors and capable of operating in either step-up or step-down mode. The converter system output is controlled by a controller whose main function is to operate the switching devices in a converter system and maintain a regulated output. The control technique plays a very important role in switched mode power converter. This research focuses on buck and boost converters.The converters are modeled, designed, constructed and analyzed for their closed loop performance.

1.1.1 Performance Evaluation of Switching Converters

The converters are tested for following power quality parameters

1. **Input Voltage Range:** The input voltage range determines the maximum and minimum allowable input supply for the converter. Input supplies higher than the maximum allowable input can damage the converter.

2. **Maximum Output Current:** It is the maximum output current that the converter can provide for the regulated voltage.

3. **DC Line Regulation:** DC line regulation is defined as the resulting change in the output voltage for a given change in the input voltage.

4. **DC Load Regulation:**The DC load regulation is the change in output voltage for a static change in output (load) current.

5. **Efficiency:** The efficiency is defined as the ratio of output power to input power. The efficiency depends on the internal losses of the converter.

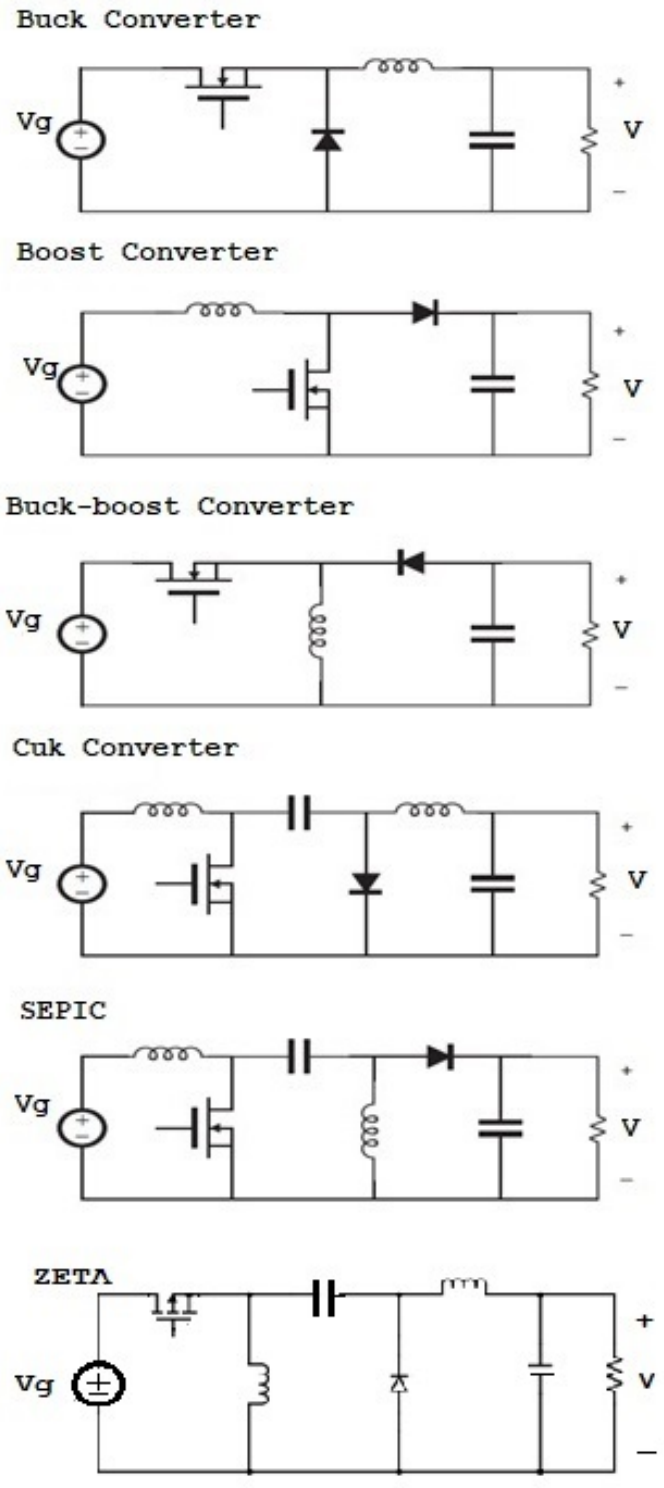

Figure 1.1: Basic types of converter

1.1.2 Necessity of Controller

The performance of a switching converter is dependent on the control strategy used. Controller plays an important role in regulating the output and achieving power quality of switching converters. The main component of a DC-DC converter is the controller. There are two types of control possible analog control and digital control. The digital control is widely used control over analog control. Advantages of digital control are as follows:

1. Digital controllers have immunity to noise.
2. They are less susceptible to component ageing and environmental variations.
3. They have improved sensitivity to parameter variation.
4. They have ease of integration with other digital systems.
5. Ability to implement sophisticated control schemes by means of programming.
6. They have low power consumption.

In DC-DC converters, the average output dc voltage needs to be controlled to a desired level. This control is achieved by controlling the on-off duration of the switches. Switched mode DC-DC converters utilize one or more switches to transform dc from one level to another. There are two methods to achieve it.
1) Constant frequency switching and adjusting the on time of the switch. Also called as pulse-width modulation(PWM) method,
2) Both switching frequency and on time of the switch are varied.

The PWM switching is widely used method as shown in figure 1.2. The control voltage is obtained by amplifying the error which is the difference between the actual output voltage and its desired reference value. The switch control signal is generated by comparing $V_{control}$ with a repetitive waveform which is a saw tooth wave. The frequency is kept constant and is chosen to be in a few kilohertz to a few hundred kilohertz range. The average value of the output voltage depends on ton and toff. When the amplified error signal, which varies very slowly with time, is greater than the saw tooth waveform, the switch control becomes high, causing the switch to turn on. When the error signal is less than the saw tooth waveform, the switch turns off. The frequency of the repetitive waveform with a constant peak, establishes

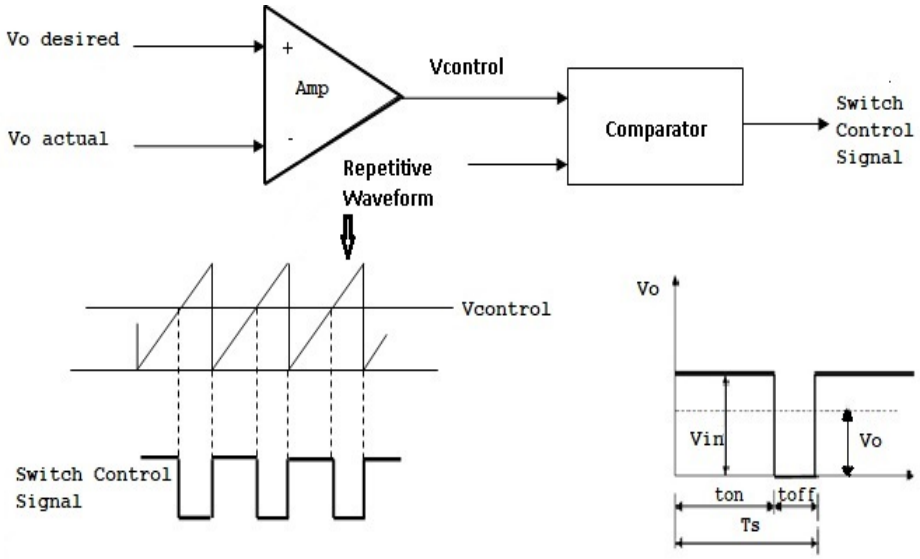

Figure 1.2: Pulse Width Modulation

the switching frequency. In PWM method, a constant frequency is employed and the on time of the switch is adjusted to control the average output voltage. Thus, the switch duty Ratio D which is the ratio of the on duration to the switching time period is varied.

The other control method where in both on time and the switching frequency is varied has drawbacks of ripple components in the input and output waveform of the converter.

1.1.3 Non linear Characteristics

Chaos is a kind of quasi-stochastic behaviors of determinate nonlinear system. DC–DC converters are typical nonlinear systems because of their switching processes. Some irregular behavior, such as sub harmonics and intermittent instability, has been observed in practice. The PWM switching is widely used method in DC-DC converters. Studies suggest that this type of switching leads to chaos. The method used to analyze chaos is bifurcation, which describe the changes in system behavior as a parameter is varied.

1.1.4 VLSI Design Technology-FPGA Platform

Very large Scale Integration (VLSI) Design technology implements more than 10k transistors integrated on silicon chip(IC). It is one of the basic components of today's high technology. VLSI devices are found in all applications from simple household appliances to complex aircrafts. The advantages are smaller size, lower cost, lower power, higher reliability and

more functionality. VLSI family consists of Programmable Logic Devices (PLD's) and Application Specific Integrated Circuits (ASIC).
The PLD's are further classified as

1. Field Programmable Gate Arrays (FPGAs)

2. Complex Programmable Logic Devices (CPLDs)

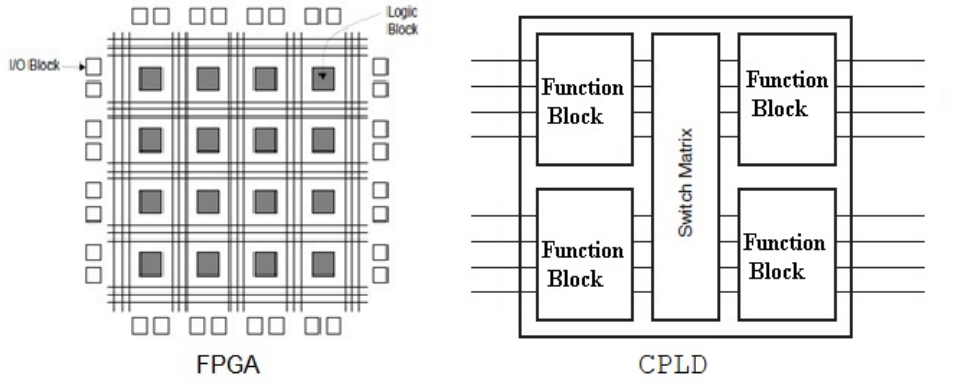

Figure 1.3: Programmable Logic devices

Figure 1.3 shows the structure of a FPGA and CPLD. FPGA's have logic blocks which are programmable. They can implement combinational as well as sequential logic. These blocks can be interconnected via a programmable interconnect. There is a periphery of programmable input output cells surrounding the core. CPLD has function blocks which implement the logic. They are connected by a switch matrix which is programmable. The function blocks and the the switch matrix are connected to the input output blocks. ASIC are specific IC's which can be produced in bulk once the PLD's are tested to satisfy the requirements. The prototype is designed on PLD which can be easily programmed using a bit file generated from the software.

1.2 Organization of the Report

The organization of the report is as follows.

- Chapter 2 comprises of extensive research on the various types of control strategies for switching converters and different platforms for controller, VLSI based controllers and their various approaches to design and nonlinear control of converters wherein chaos

and the bifurcation theory are studied for DC-DC converters.It identifies the research gap and states the research objectives

- Chapter 3 discusses the buck converter, its working, modeling, frequency and time domain analysis for various types of controllers. Design and implementation of buck converter and testing FPGA based PI and PID controllers is discussed and performance is evaluated.

- Chapter 4 discusses the working, modeling and design for boost converter. The hardware is tested with the FPGA based controllers and performance is evaluated.

- Chapter 5 discusses the FPGA platform and the various methods of modeling. The closed loop is implemented on the FPGA using a FSM approach. The controller and the various blocks of control loop are designed, implemented and tested on a inbuilt logic analyzer. The device utilization for PI and PID controllers using Xilinx FPGA is obtained.

- Chapter 6 discusses nonlinearity in converters, chaos analysis for buck and boost converters. The iterative maps are derived and the simulations are performed to obtain bifurcations diagrams and phase portraits.

- Chapter 7 summarizes the research conclusions and discusses the future scope.

Chapter 2

Literature Review

A DC-DC converter is an electronic circuit or electromechanical device that converts a source of direct current from one voltage level to another. It is a type of electric power converter. Power levels range from very low (small batteries) to very high (high-voltage power transmission). A complete review of DC-DC converters, digital control methods, FPGA based control and applications, FPGA based discrete controllers and non linear analysis of converters is been placed.

2.1 Switching Converters

Converters employ switched mode devices and passive components like inductors and capacitors to regulate the output. The switched mode technology has reached a matured level for improving power quality in terms of power-factor correction (PFC), reduced total harmonic distortion at input ac mains and precisely regulated dc output in buck, boost, buck-boost and multilevel modes with unidirectional and bidirectional power flow as discussed in [5]. A complete survey of improved power quality converters is carried out by Bhim Singh et al [5] wherein different types of converter topologies, methods of control, design features, selection of components, suitability for certain applications are discussed. Various control techniques are used to get fast output response and high level of power quality at input ac mains and dc output. The control is implemented in three parts.

1. The important variables like the supply voltage, supply current, output voltage, inductor current, capacitor voltage are sensed and scaled to the required processor in the first stage. The sensing can be done by sensors. The scaling is done by CT or PT. Normally an ADC is required to convert the data for the controller.

2. The second stage is the actual controller with a control algorithm. These can be Analog controllers, low cost microcontroller, DSP or an ASIC. This depends on the rating, cost, customer requirements and the type of converter used. The control approach can be PI, PID, sliding mode, neural, fuzzy, adaptive control. Normally the output voltage of the converter is fed into these controllers to get the desired control.

3. The third stage is to derive the gating signals for the solid state devices. The controller output is compared with a reference signal to generate the required pulses. The design of this feedback is a important feature for fast response and improving the transient and steady state characteristics of the converter. The gating signals are fed through an optocoupler for isolation and then amplified to the desired value of the power devices.

Self Commutating Devices with high switching rates are used as switching devices. Mosfet's, IGBT, GTO are suitable for high switching rates with low, medium and high power ratings respectively. Many low cost, high volume dedicated IC's are available to control these converters. Measurement equipments like power analyzers, power scopes, power monitors, and spectrum analyzer are useful to find the factors like harmonic distortion, power factor, crest factor, ripples, and surges of the converter. Dedicated processors and ASIC's development for power converters are used because of low cost, ease in control, compact and high speed.

Switching converters are modeled using various methods like mathematical model, circuit, transfer function and state space approach. State space approach has advantages like compact representation of equations and ease of obtaining ac and dc transfer functions. Tan and Hoo [6] model and simulate the DC-DC converters in Matlab/Simulink using the state space block.

2.2 Digital Control methods

Yan-Fei Lin et al. [7] present an overview on advances in digital control. The converters considered are low to medium power AC-DC switching converters. The paper discusses the challenges to digital control. It also presents the research in online efficiency optimization, controller auto tuning and nonlinear control. Digital design techniques are reviewed. One of the basic technique is analog to digital design of the compensator. This is possible by either

backward Euler's method, Bilinear Transformation, Pole Zero Mismatches. But the drawbacks are discretization effects, delays associated with acquisition, computation and zero order hold. A small signal discrete model is analyzed. The delay time in the control loop can be related to the zero of the transfer function of control to output. The poles are unaffected. Also the equivalent series resistance (ESR) of the output capacitor does not add another zero. This zero is shifted opposite to the delay time. A direct digital method is discussed which can be useful in the implementation of a PID compensator. The computational delay in a multiplier can be reduced by a LUT or bit shifting. The current-programmed control presents a challenge to digital control. Methods of inductor current sampling have been discussed. The ideal is the mixed-signal controller which gives a faster response with added cost of control .The third part of the control strategy is the Digital Pulse Width Modulator(DPWM). The problem of Limit cycle oscillation (LCO) is associated with the quantization effects of the ADC and DPWM. High gain of the compensator integrator or very coarse quantizing step of the DPWM is the main reasons for LCO. Methods like tapped delay lines. Ring oscillators and hybrid DPWM techniques are reviewed. The PMBus interface has improved the power management communication and system level integration of controllers. Digital control is also used to adjust the parameters of the controller so that the efficiency is optimized. The switching losses in the converter can be reduced by control. Autotuning methods are reviewed. Digital control also helps in non linear and charge balance control which improves the dynamic response of the converter. Thus the advantages of Digital Control over analog control have been discussed.

K.N.Hasan et al. [8] describe a comparative study of current control methods of switch mode converters for photovoltaic applications. Average current control, hysteresis current control, current programmed control and nonlinear carrier control methods are discussed considering the input variations and load changes of a PV system. The current controllers are simulated in MATLAB/Simulink. A PV system is modeled and transient response and power quality issues like THD are compared for all the control strategies. The study concludes that all the current control methods can be implemented depending upon working conditions.

Hrishikesh Nene [9] presents a microcontroller based implementation of a controller for a DC-DC converter in automotive applications. There are two directions of power flow required—one high voltage bus to low voltage battery in the buck mode uses phase shifted full bridge(PSFB) with synchronous rectification and reverse mode is in the boost mode with

a push pull stage. Peak current mode control of PSFB with adaptive zero voltage switching is implemented for buck converter and voltage control mode and average current control mode is implemented for boost converter. With the help of digital control, various control schemes are implemented on the same hardware. The modes of operation are defined for various controls. All operating modes are simulated and tested for a 600W system .The advantage of digital control is discussed.

Pallavee Bhatnagar et al. [10] present design of a DC-DC converter for a PV application using two control strategies. The converter is simulated for a switching frequency of 100 KHz using PWM control and hysteresis control. The PV array is simulated on SimScape software. The design of boost converter is explained. The output waveforms for voltage, current, inductor current, diode current are plotted for both types of controls. Both the controls are discussed with their advantages and disadvantages.

Souvik Chattopadhyay and Somshubhra Das [11] propose a digital current mode control technique for DC-DC converters. The inductor current is sampled only once in a switching instance. The slope of the ramp is determined analytically on the steady state conditions and hence there is less load of computation of the controller. The configuration of the DPWM for implementations of all the three variations of current-mode control, namely peak, average, and valley current-mode controls, has been proposed. The results are validated and implemented on TI's general purpose DSP starter kit.

Wang et al. [12] propose a controller for DC-DC switching converters used in battery powered hand held devices. Two modes digital pulse width modulator (DPWM) and an all digital pulse frequency modulator (DPFM) are discussed Advantages of DPWM are operation in high constant switching frequency whereas DPFM operates with low power consumption with control over switching frequency. An experimental FPGA prototype and an application specific IC (ASIC) are built for a low power buck converter and verified. The power is validated on 0.18um CMOS process. The DPWM architecture is modified from the conventional by an absence of external clock. A ring based segmented architecture is employed wherein the 2 blocks of 16 delay lines are connected to two multiplexers A and B. The logic is generated by the data lines selecting Mux A and Mux B. The hardware for DPWM is reduced with the ring oscillator. The DPFM architecture is race based with three blocks DPWM, End of Race (EOR) and DPFM.

Saggini et al. [13] describe an innovative method of designing a low-complexity, high-

performance digital controller based on different design strategy of current programmed control and variable frequency operation. The controller employs only two digital-to-analog converters (DACs) with low resolution, thus having a considerable resource saving. The control algorithm has been implemented into a commercially available FPGA device and tested on a prototype four-phase buck converter. The results are validated after experimentation.

A continuous time digital controller is designed by Zhenyu Zhao and Aleksandar Prodic [14] in which the sampled time is continuous and the amplitude is digitized. The application is a low-power, high frequency DC-DC switch-mode power supply. It controls both the transient and the steady state response. During transients it utilizes a fast voltage recovery mechanism based on the real time processing of output in digital domain. In steady state it is a conventional pulse width modulator. The processor consists of a set of asynchronous comparators, delay cells, and combinatorial logic. A capacitor charge balance algorithm is implemented which is based on the detection of the output voltage peak /valley point, thus eliminating the current measurement. It is experimented on an FPGA and tested with a low-power dc–dc converter operating at 400-kHz switching frequency. The fast recovery time is limited by the values of inductor and capacitor

A digital controller for an electric vehicle has been designed by Seung-mo Kim [15] which implements PI control and sliding mode control. It has Zero voltage switching and Phase shift full bridge topology. For voltage control PI is used and for protection from over current, over voltage sliding mode is used. It is implemented with a microcontroller and tested for a 13.7V, 130A Dc output.

S.Vijayalakshmi ,K.Muthukumar [16] presents a sliding mode controller for DC-DC converters. The converter design is based on large signal model eliminating stability issues. A MATLAB/Simulink environment is used for design and simulation of closed loop synchronous buck converter in [17]. PID and auto tuned PID(AT PID) controller are designed and simulated. Transient response is analysed. The closed loop control simulation is helpful for FPGA or ASIC implementation,.

2.3 FPGA based control

FPGA's are programmable logic devices. The technology used to program a FPGA is the with the SRAM memory. An FPGA is defined as a matrix of configurable logic blocks

surrounded by a programmable interconnect structure. Programmable input output pins surround the core. FPGA based controllers implemented on a VLSI platform have high degree of parallelism and concurrency. E. Monmasson, L. Idkhajine and M. W. Naouar [18] discuss the FPGA platform for controllers design and its advantages. FPGAs are frequently used to implement complex functions due to recent advances in very large scale integration (VLSI). Design tools and methods are developed based on hardware description languages (HDLs) such as very high-speed integrated circuits (VHSICs) HDL (VHDL) and verilog. In addition IEEE standards are developed which aid in the development of these description languages in the field of microelectronics. Thus HDL can be designed at various levels of abstraction - system level, behavior level, RTL level and physical level. The main steps of FPGA based controllers are discussed in [18] which include the modular design, HDL coding, functional simulation, synthesis, physical design i.e partitioning, floor planning, routing and finally downloading on to FPGA chip. The design methodology can be implemented with different architectures using hardware description language(HDL) [18] or a Matlab Simulink environment with system generator tools [19]. A look up table(LUT) based and a multiplier based controller is designed on FPGA with area and power utilization as the constraints in [19].It gives a FPGA based PID controller for converter applications. The Proportional-Integral-Derivative (PID) controller is one of the most common types of feedback controllers that are used in dynamic systems. Matlab/Simulink environment is used for the PID controller design to generate a set of coefficients associated with the desired controller characteristics. These controller coefficients are then included in VHDL that implements the PID controller on to FPGA. Two architectures of PID controller are considered- multipliers and LUT based with their device utilization and power dissipation reports to show the resource utilization and power dissipation of selected FPGA. The architectures are implemented in FPGA Virtex-5(ML505) XC5VLX50T-1FF1136 (-1 speed grade) device Various papers have been reviewed with FPGA based control for DC-DC converters.

Miro Milanovic et al. [20] have designed a FPGA based PI controller for a DC-DC buck converter. An analog to digital converter, digital PI controller and PWM module are implemented on an FPGA. The controller design is carried out with various resources available on FPGA. A successive approximation based A/D converter is designed and implemented on FPGA. The comparator and integrator are external to the FPGA. The PI controller and the pulse width modulator are also implemented on FPGA. The output is a digital pulse

which can be given to the switching device of the converter. The response of the controller is validated. It describes a possibility of digitized control for a buck converter.

A PI controller is designed using a modular approach of datapaths and sequential paths in [21] which are controlled by a finite state machine. A comparison of a digital pulse-width modulator (DPWM) and a digital pulse-frequency modulator (DPFM) is performed in [22]. It implements the control loop on an ASIC 0.18um process with a controller operating in a DPWM operating at high frequency and DPFM featuring low power consumption. A complete programmable digital IC is designed and implemented for high switching frequencies in [23]. The said configuration has low silicon area, low power consumption and less complex logic as compared to an analog IC. Implementation has an ADC with delay line, LUT based digital compensator and a hybrid DPWM block. The VHDL design is tested on an ASIC of 0.5um technology. However, the design is implemented for high frequency of 1MHz. FPGA based control is implemented taking into consideration three main rules for design as described in [24]. They are simplification of the algorithm called refinement, using a modular approach for design and compatibility between the design and hardware. FPGA platform is used in [25] for testing and verifying different DC-DC converter topologies, control modes and switching frequencies, including a synchronized load change mechanism and a build-in acquisition memory and host interface for easy configuration,

A flexible experimental FPGA based platform for testing and verifying different DC-DC converter topologies, control modes and switching frequencies, including a synchronized load change mechanism and a built-in acquisition memory and host interface is presented in [25]. The controller is implemented on Xilinx Spartan 6 FPGA partly in pure logic and partly in a softcore microprocessor as a System-on-Chip solution (SoC). Each of the logical modules are implemented with low coupling between the modules for easy update of functionality.

Pulse width modulator is the basic block in the closed loop control. Two structures of high resolution digital pulse width modulator (DPWM) control circuit are discussed in [26]. Embedded digital clock manager (DCM) blocks and digital programmable delay circuits are employed as the basic resources to construct the field-programmable gate array (FPGA)-based DPWM implementations. The implementation is done on the Artix-7 FPGA device by Xilinx. For frequency of 200 MHz, the resolutions of the two structures are 625 ps and 500 ps, respectively.

Shettar et. al [27]proposes another digital PWM architecture for DC-DC Converters. This architecture includes a DCM block for improving the switching frequencies. Gray counter and one hot encoder circuit logic is implemented for low power consumption. With the counter bits zero, the enable logic is made high which turns on the one-hot encoder thus acting as the reset pin for it. Thus the one-hot encoder circuit is on only when required thus reducing the switching power. The MSB output of the one-hot encoder is given to the set pin of the RS flip-flop. Depending on the requirement of the duty cycle, the PWM control circuit resets the flip-flop thus producing a variable duty cycle. Xilinx 14.2 and ISim simulator is used for simulation.

2.4 FPGA based discrete controllers

A digital PID controller is designed and simulated in Matlab using re-design approach in [28]. For a desired loop gain, crossover-frequency and phase-margin, digital filter direct form based PID controller is implemented. Mapping from analog to discrete domain is done by backward Euler method.

Different types of digital controllers, their design, tuning and frequency domain analysis is discussed in [29] [30] [31]. Compensator design for PI,PI with lead, lead,and PID is carried out in [32]- [37].

FPGA based PID controller hardware is shown in figure 2.1. It implements the discrete PID equation given by [38]

$$u[k] = u[k-1] + q_0 e(k) + q_1 e(k-1) \tag{2.1}$$

PID controller implementation on FPGA is also discussed in [39]. It utilizes three combinational logic multiplier, one subtractor three adders and three registers blocks. The method of ADC FPGA interfacing is discussed. Hardware software co-simulation model of PID controller using Matlab System Generator tools is implemented for a buck converter in [40] [41]. The hardware code is generated by the Matlab HDL coder which can be implemented on a FPGA. PID controller is implemented using the finite state machine (FSM) in [42]. This approach separates the data path and the sequential logic and is very useful for the PID controller. The controller triggers each state on a clock and thus the output is calculated.

FPGA software Vivado has its own simulation sub-systems making it possible to check the output. Three types of simulations are available- functional simulation, simulation after

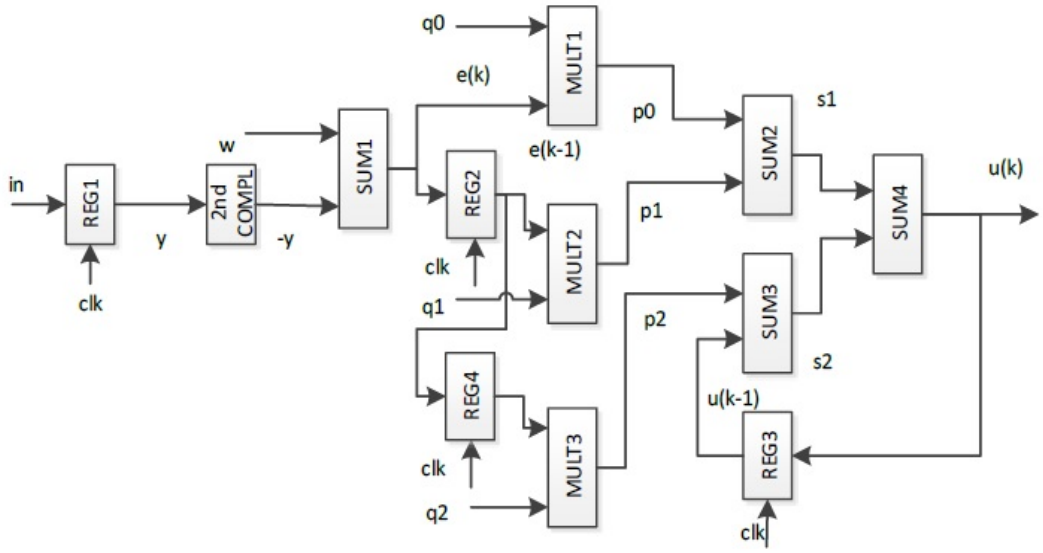

Figure 2.1: Parallel architecture of Discrete PID for FPGA design [38]

synthesis and time simulation. A discrete PI controller is implemented in [43] using Xilinx Artix-7 FPGA. PID implementations on FPGA using floating point and fixed point representations are discussed in [44]. Shorter design cycles and resource savings is achieved in fixed point implementations. Thus discrete controllers on FPGA can be designed with behavior, parallel or FSM structure and are implemented with HDL coding or Matlab Simulink HDl coder.

2.5 Non Linear performance of switching converters

All power electronic circuits have the following properties:

- Switches make the circuit toggle between two or more different topologies, continuous conduction and discontinuous conduction with different sets of differential equations.
- Inductors and capacitors are the storage elements (inductors and capacitors) which absorb energy from a circuit, store it and return it.
- The switching times are nonlinear functions of the variables to be controlled (mostly the output voltage).

Thus,the feedback controlled switching is the basic source of non linearity in power electronic circuits. In addition there are nonlinearities present in the switches, storage elements

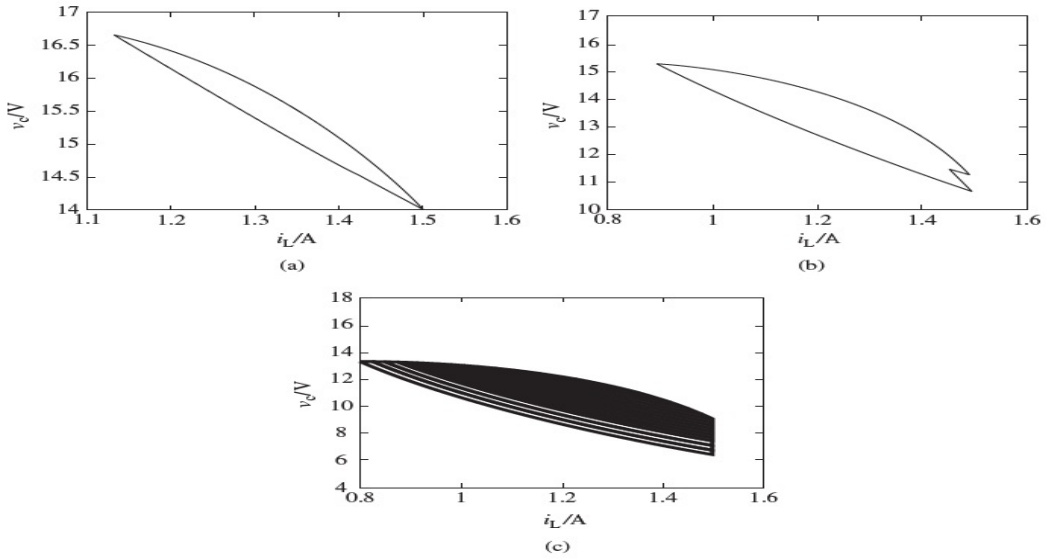

Figure 2.2: Phase portraits of (a) period-1, (b) period-2, and (c) chaos. [47]

and the electromagnetic couplings between components. However, the main source of nonlinearity is the switching element, which makes power electronic systems nonlinear even if all components are assumed to be ideal. [45]

DC-DC converters exhibit bifurcation and chaos if switching action is governed by feedback control as observed in regulated power supplies. The cyclic switching operation and reactive components give rise to a variety of nonlinear behavior like bifurcation and chaos. Chaos in power electronics has been an area of intensive study for the last many years.Studies of the nonlinear behavior of power electronic converters began with DC–DC converters over the past 30 years. In 1984, the chaos phenomenon of the buck converter was first mentioned by Brochett and Wood. Hamill and Jefferies [46] introduced bifurcation and chaos in a PWM buck converter, where the difference equations and return maps were utilized to analyze its stability domain in 1988. The phenomena of boundedness, intermittency, and chaos were then observed in an experiment by Krein and Bass in 1990. [47]

A phase portrait is a collection of trajectories that represents the solutions of equations in the state-space. Figure 2.2 gives the example of phase portraits for period-1, period-2 and chaos. A qualitative change in the number of solutions to a dynamical system by varying a parameter is called a bifurcation. A bifurcation diagram is a graphical representation of bifurcation [47]. A parameter is varied and plotted along the x-axis, and the asymptotic behavior of a sampled state variable is plotted on the y-axis as discrete points. A bifurcation diagram of a boost converter is shown in figure 2.3. If the system is operating in period-l

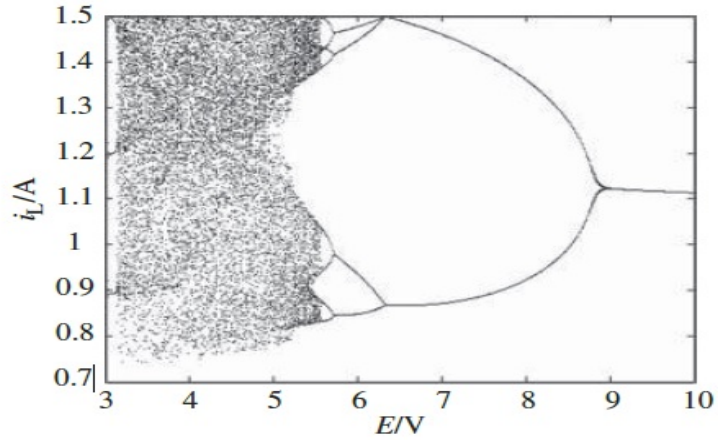

Figure 2.3: Bifurcation diagram of boost converter [47]

for some parameter values corresponding to a cycle in the phase portrait, there will be only one point in the bifurcation diagram. If it is in period-2, there will be two points. Such a bifurcation diagram summarizes the change in system behavior in response to the variation of a parameter.

Methods for controlling chaos in nonlinear systems can be classified into two general categories, namely, feedback control methods and non-feedback control methods. Feedback methods include the Ott-Grebogi-Yorke (OGY) method, Variable Ramp Compensation (VRC), Time-Delayed Feedback Control (TDFC) method. Examples of non-feedback methods include adaptive control, Resonant Parametric Perturbation (RPP). Based on the bifurcation analysis and parameter adjusting, the most simple chaotic control method is by changing the system parameters. G. Poddar, K. Chakrabarty, and S. Banerjee [48] propose two new methods for power electronic converters having a pulse width modulated (PWM)feedback controller.

The methods take advantage of the existence of unstable periodic orbits in the strange attractor, as in the OGY method. However, the OGY method stabilizes the unstable fixed points of two dimensional maps by applying small perturbations to push the state towards the stable manifold. The first method controls chaos by targeting the unstable fixed points in every cycle. The control force is calculated by making use of the linear character of the system between switching instants simplifying the control logic. The second method stabilizes the systems in the unstable periodic orbits by small changes in the switching-on instant in every cycle. The state variables corresponding to the unstable fixed points are stored in the memory registers which decide the switch-on instants. They are particularly

suited for switched linear systems and power electronic circuits as they have the advantage of the piecewise linearity and switching behavior

Analysis of DC-DC buck converters with PWM control is carried out in [49] in the one-periodic and two-periodic orbits which cross the voltage ramp once per cycle. Their stability is observed by computing the characteristic multipliers associated with each one. Sub-harmonics, bifurcations, and the presence of a strange attractor are also discussed. A plot of the number of crossings in the ramp is plotted.

DC-DC buck converters are analyzed for bifurcation and chaos in [50]. The nonlinear phenomenon are classified into standard bifurcations like, flip, Hopf and saddle node bifurcations. Analytical tools along with numerical simulations are used to predict the bifurcation phenomena. All current mode controlled elementary converters, PWM voltage mode controlled converters undergo flip bifurcation and sub harmonic oscillations when a control parameter is varied.

Chaos and bifurcation behavior of buck converter is analyzed with voltage mode and current mode control using discrete iterative map in [51]- [61]. The methodology used to obtain the non linear analysis is as follows

1. Mathematical modeling is perform to obtain the equations for inductor current and capacitor voltage.

2. The inductor current/capacitor voltage is plotted for variation of input voltage and reference parameter- it will be current for a current mode control and voltage for voltage mode control. These are the bifurcation diagrams.

3. Phase portraits which are inductor current and capacitor voltage plots are obtained.

4. The period-1, period-2 values are simulated individually to obtain the chaotic behavior of inductor currents and capacitor voltages.

The peak inductor current is taken as the control parameter. Matlab simulation is used for bifurcation diagrams in [51] [52].Matlab and Pspice simulations are used in [53]. PID control and Integral Absolute Error (IAE) are used as adaption coefficients to control chaotic behavior, and particle swarm optimization (PSO) and the genetic algorithm are used to find the optimal gain parameters for the PID controller. [54] also simulate bifurcation behavior in buck converter using PSpice. A valley inductor current is taken as a control objective for

valley current controlled buck converter in [55]. As the minimal value of I_{ref} is zero and whenever the inductor current ramps down the switch S1 will be turned on and inductor current will ramp up, valley current controlled buck converter cannot operate in discontinuous conduction mode. Therefore, the inductor current never falls to and remains at zero and valley current controlled buck converter is kept working in CCM. Discrete time map is derived in [56] using discontinuous mode of operation(DCM) of a buck converter. A proportional feedback is considered. The control variable is capacitor voltage and the iterative equation is in terms of duty cycle and the feedback factor. For different values of the feedback factor, the output voltage exhibits period-1, period-2, period-4 and chaos.

A. Mehrizi-Sani, W. Kinsner, and S. Filizadeh [57] study the DC-DC buck converter with constant-frequency pulse-width modulation feedback control in continuous conduction mode. Phase-space and time-domain plots for several periodic and chaotic orbits are plotted. The bifurcation diagram is studied together with periodic orbits and chaotic behavior of the circuit.A method for computation of Lyapunov exponents in discontinuous systems is implemented.

In addition to reference voltage and the input voltage as the control parameter, additionally the load resistance is taken as a control parameter for a forward converter in [58]

Boost converters with different configurations like single module, two module, PFC boost are studied for chaos and chaos control in [59]. The methodology to iterate the boost converter to obtain the bifurcation is explained.

Discrete iterative map for boost converter is derived and the bifurcation and chaos is simulated in [61]. In the above mentioned references, the research is the study of chaos and the means of controlling chaos. However, research is now beginning to move towards uses for chaos. The major application is the possibility of improvement of EMC by chaotic spread spectrum techniques, targeting and control of chaos in switched mode power supplies and the increased agility of converters that are operating on the edge of stability.

David C. Hamill, Jonathan H.B. Deane and Philip J. Aston [62] suggest applications for chaotic power converters using the peak current controlled boost converter. A possible method of using chaos to improve the electromagnetic compatibility (EMC) of power supplies is proposed.

2.6 Research gap and objectives

Literature has numerous converters with different types of controllers. Various platforms are available to implement digital controllers. Control techniques are implemented using microcontrollers, neural networks, fuzzy logic, digital signal processing (DSP) and very large scale integration (VLSI).

In the literature, it is observed that the controllers are with a LUT or a Multiplier based architecture. Finite State Machine(FSM) based PI/PID controller using VHDL language is not implemented. The control loop with the controller and pulse width modulator operating in real time is required. Frequency, time domain analysis of controllers and non linear analysis with chaos and bifurcations study is lacking. A versatile FPGA based controller which can be used for a low frequency DC-DC switching converter needs to be developed. Identifying this as research gap, designing and implementing a VLSI based controller for optimal control of a DC-DC converter and analyzing its performance is the main goal of this research. Since VLSI technology has numerous advantages over other platforms in terms of size, speed and power, this research implements a digital controller on a VLSI platform using FPGA as a device. There are various types of controllers. Linear controllers viz. PI (proportional integral) and PID(Proportional integral and derivative) are the most widely used controllers. They are analyzed for frequency domain to improve the phase margin and time domain analysis to improve the transient and steady state response.The research objectives are further divided as follows.

1. To study the various types of controller strategies implemented for switch mode converters.

2. To model, design, implement a buck converter and boost converter and test the converters with the proposed controller.

3. Design a FPGA based PI controller and PID controller using hardware description language. To simulate and test the controllers on FPGA using real time logic analyzer.

4. To analyze buck and boost converters for chaos using iterative map and obtain the bifurcations.

2.7 Conclusion

DC-DC converters with different topologies are used for applications like PV control, switch mode devices and electric vehicles. Current mode, voltage mode control methods with different types of controllers viz.PI, PID, sliding mode are reviewed. Advantages of FPGA platform for control are compact design, parallel architecture, high speed and low cost. FPGA based digital controllers are developed using Xilinx, Altera and Matlab-Simulink HDL environment. Finite state Machine(FSM) based controller for low frequency DC-DC switching converter needs to be developed. Various research papers in this area are reviewed. The nonlinear analysis also plays a important role in DC-DC converters. Chaos and bifurcation analysis for DC-DC switching converters is studied. The research gap is identified and the research objectives are stated.

Chapter 3

Buck converter with proposed Controller

3.1 Introduction

A buck converter is a step down converter. It steps down the input voltage in order to achieve a desired output. Buck converters are used in regulated dc power supplies, cellphones, PCs and laptops, battery chargers, solar chargers and power audio amplifier. Buck converters also find applications in motor speed control. They are designed to have an efficiency of 90% or higher thus resulting in low power loss. The main components of a buck converter are switch, diode, inductor and a capacitor. The switch is controlled by a control signal generated by a controller. The controller maintains the constant output voltage of the buck converter. In this chapter, the working of a buck converter is discussed. Converter transfer functions are derived using state space modeling approach. The converter design using the design equations is placed. Closed loop simulations are performed with different compensators using Matlab Simulink. The frequency and time domain analysis is obtained for the different types of compensators. Hardware implementation with the components and the proposed VLSI based controller is tested for voltage regulation and performance is evaluated.

3.2 Buck converter working principle

A buck converter is shown in figure 3.1. The input voltage source V_{in} is connected to a controllable solid state device S which operates as a switch. The solid state device can be a power MOSFET, BJT or a IGBT. The switch is controlled by a control signal given at the gate source voltage of the MOSFET. By varying the duty ratio of the switch, the output voltage can be controlled. A low-pass LC filter is designed to reduce the output voltage

fluctuations. The load is assumed to be purely resistive load. The stored inductive energy is dissipated through the diode D when the switch is off.

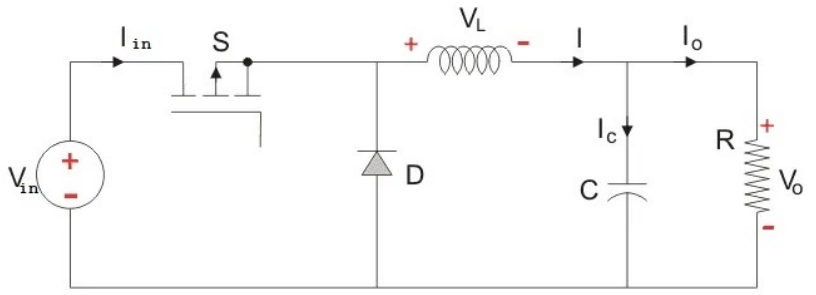

Figure 3.1: Buck converter

The controlled switch is turned on and off by using Pulse Width Modulation(PWM) control signal. There are two types of PWM i.e time based and frequency based. A wide range of frequency is required for frequency based PWM which complicates the design of inductor and capacitor. Hence it is not widely used. Time based modulation is mostly used for DC-DC converters. It is simple to construct and use. The frequency remains constant in this type of PWM modulation. The buck converter has two modes of operation. The first mode is when the switch is on and conducting as shown in figure 3.2(a).

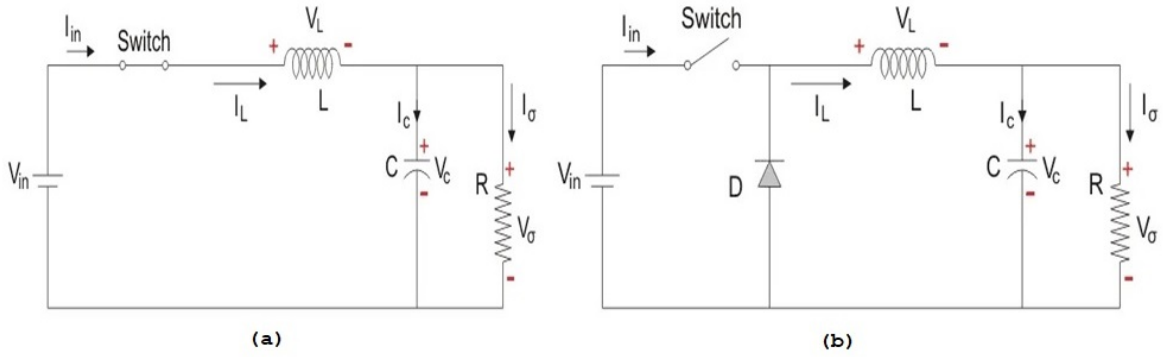

Figure 3.2: Buck Converter working (a) Mode 1:switch closed (b) Mode 2:switch open

The current flows through the switch and the inductor and capacitor. The diode does not conduct and the voltage across the capacitor in steady state is the output voltage The switch is on for a time T_{on} and is off for a time T_{off}. The time period T is given as

$$T = T_{on} + T_{off} \tag{3.1}$$

and the switching frequency f_s as

$$f_s = \frac{1}{T} \tag{3.2}$$

The duty cycle D is defined as

$$D = \frac{T_{on}}{T} \tag{3.3}$$

Analysis in steady state is done using KVL

$$V_{in} = V_L + V_o = L\frac{di_L}{dt} + V_o \tag{3.4}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT} = \frac{V_{in} - V_o}{L} \tag{3.5}$$

$$\Delta(i_L)_{closed} = \frac{V_{in} - V_o}{L}DT \tag{3.6}$$

The second mode is when the switch is open as shown in figure 3.2(b) When the switch is open, the energy stored in the inductor is dissipated in the load resistance, and this helps to maintain the flow of current through the load. Analysis the circuit in Mode 2 by applying KVL.

$$0 = V_L + V_o = L\frac{di_L}{dt} + V_o \tag{3.7}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{-V_o}{L} \tag{3.8}$$

$$\Delta(i_L)_{open} = \frac{-V_o}{L}(1-D)T \tag{3.9}$$

The net change of the inductor current over anyone complete cycle is zero.

$$\Delta(i_L)_{closed} + \Delta(i_L)_{open} = 0 \tag{3.10}$$

Substituting the values,

$$\frac{V_{in} - V_o}{L}DT + \frac{-V_o}{L}(1-D)T = 0 \tag{3.11}$$

$$\frac{V_o}{V_{in}} = D \tag{3.12}$$

The inductor voltage and current with respect to time is as shown in figure 3.3. The region A is for the continuous conduction when the switch is closed and region B is for the discontinuous mode when the switch is open. The inductor current peaks at the boundary between the continuous and the discontinuous mode and goes to zero at the end of the period. At this boundary the average inductor current I_{LB}, where the subscript B refers to the boundary is given by

$$I_{LB} = \frac{1}{2}I_L = DT\frac{V_{in} - V_o}{2L} = I_{oB} \tag{3.13}$$

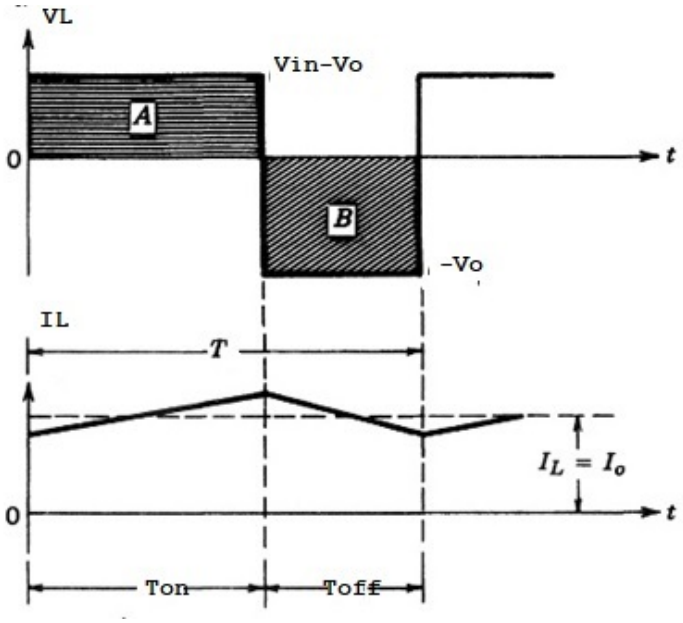

Figure 3.3: Voltage current characteristics of buck converter

Thus if $I_{oB} < I_{LB}$, then the inductor current becomes discontinuous.Figure 3.4 shows the current at the boundary conditions. Assuming the input voltage V_{in} to be constant during

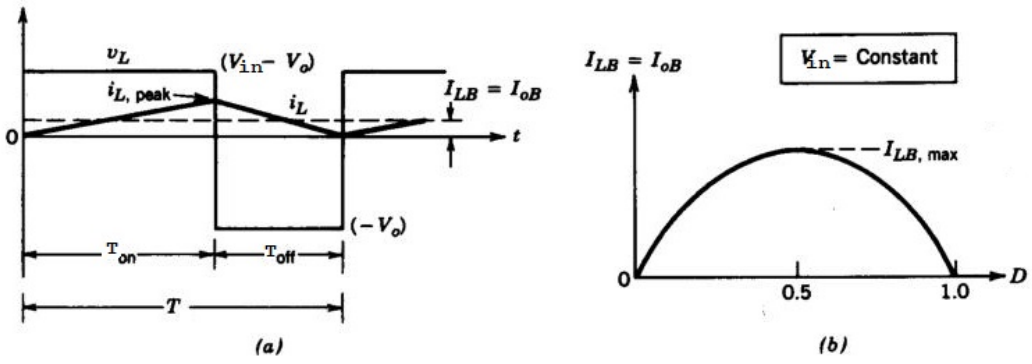

Figure 3.4: Boundary conditions of inductor current

the converter operation, I_{LB} as a function of duty ratio D is shown in figure 3.4. The output current required for continuous conduction mode is maximum at D = 0.5

$$I_{LB,max} = \frac{TV_{in}}{8L} \tag{3.14}$$

The ripple in the output voltage is calculated assuming that all of the ripple component in I_L flows through the capacitor and its average component flows through the load resistor ΔQ. Therefore, the peak-to-peak voltage ripple ΔV_o can be written as

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{\Delta I_L T}{8C} \tag{3.15}$$

Substituting the value of ΔI_L,

$$\Delta V_o = \frac{V_o(1-D)T^2}{8CL} \tag{3.16}$$

Thus the voltage ripple is given by

$$\frac{\Delta V_o}{V_o} = \frac{(1-D)T^2}{8CL} = \frac{\pi^2}{2}(1-D)\left(\frac{f_c}{f_s}\right)^2 \tag{3.17}$$

where switching frequency f_s=1/T and $f_c = \dfrac{1}{2\pi\sqrt{LC}}$

The voltage ripple is minimized by selecting a corner frequency of the low pass filter less than the switching frequency i.e $f_c << f_s$

3.3 Modeling of a Buck converter

The converter is modeled using a state space averaging method. The output voltage of the converter has to be maintained constant irrespective of the changes in the input voltage and load. The duty cycle of the switch plays a very important role in regulating the output voltage at the desired reference value. Using the state space average method, the converter can be described by a single equation approximately over a number of switching cycles. Also the design can be carried out for a class of input signals like impulse, step and sinusoidal with initial conditions incorporated. The averaged model makes the simulation and control design much faster [4]. The semiconductor switch is turned on and off by a sequence of pulses with a constant switching frequency, f_s. The inductance current i_L and capacitance voltage V_o same as the output voltage are state variables. The state equations of the buck converter are obtained from figure 3.2 as follows

$$\frac{di_L}{dt} = \frac{V_{in} - V_o}{L} \tag{3.18}$$

$$\frac{dV_o}{dt} = \frac{i_L}{C} - \frac{V_o}{RC} \tag{3.19}$$

Putting these equations in the state equation given by

$$\dot{x(t)} = A_1 x(t) + B_1 V_s(t) \tag{3.20}$$

where A_1, B_1 imply mode 1 wherein switch is closed condition and i_L and V_o are the states x_1 and x_2 respectively. Substituting equations 3.18 and 3.19 in the state equation 3.20 ,we get

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_o} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_s \tag{3.21}$$

During mode 2 as shown in figure 3.2, the following differential equations are obtained

$$\frac{di_L}{dt} = -\frac{V_o}{L} \tag{3.22}$$

$$\frac{dV_o}{dt} = \frac{i_L}{C} - \frac{V_o}{RC} \tag{3.23}$$

Putting these equations in the state equation given by

$$\dot{x(t)} = A_2 x(t) + B_2 V_s(t) \tag{3.24}$$

where A_2, B_2 imply mode 2 wherein switch is open. Substituting equations 3.22 and 3.23 in the state equation 3.24 ,we get

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_o} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_s \tag{3.25}$$

The significance of state space averaging technique lies in replacing the above two sets of state equations by a single equivalent set described as follows,

$$\dot{x(t)} = Ax(t) + BV_{in}(t) \tag{3.26}$$

The A and B matrices are the weighted averages of actual matrices describing the switched system given by the following equations,

$$A = A_1 D + A_2(1 - D) \tag{3.27}$$

Substituting the values of A_1 and A_2 we get

$$\begin{aligned} A &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} D + \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} (1 - D) \\ &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \end{aligned} \tag{3.28}$$

$$B = B_1 D + B_2(1 - D) \tag{3.29}$$

$$B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} D + \begin{bmatrix} 0 \\ 0 \end{bmatrix} (1 - D) = \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} \tag{3.30}$$

The output equation is described by the following equation

$$y(t) = Cx(t) \tag{3.31}$$

where

$$C = C_1 D + C_2(1 - D) \tag{3.32}$$

hence substituting the values of matrix C, we get

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix} D + \begin{bmatrix} 0 & 1 \end{bmatrix} (1 - D) = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{3.33}$$

To solve steady state transfer ratios, the time derivatives are set to zero. Substituting it in equation 3.26, we get

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_o} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} V_{in} \tag{3.34}$$

Solving for i_L and V_o, equation is rewritten as follows

$$\begin{bmatrix} i_L \\ V_o \end{bmatrix} = - \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} V_{in} \tag{3.35}$$

Solving for the matrix inverse

$$\begin{bmatrix} i_L \\ V_o \end{bmatrix} = -LC \begin{bmatrix} -\frac{1}{RC} & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} V_{in} \tag{3.36}$$

Thus solving equation 3.36 , steady state equations are obtained

$$i_L = \frac{V_{in}.d}{R} \tag{3.37}$$

$$V_o = V_{in}.d \tag{3.38}$$

The input voltage is kept constant and duty cycle variation is to be studied. A small ac perturbation on the duty cycle (ΔD) is introduced and the resulting ac perturbations in the state variables are analyzed. The time averaged state space equation is given by

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_o} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} V_s \tag{3.39}$$

Introducing a small perturbation in D, the equation 3.39 becomes

$$\begin{bmatrix} \dot{i_L} + \Delta\dot{i_L} \\ \dot{V_o} + \Delta\dot{V_o} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L + \Delta i_L \\ V_o + \Delta V_o \end{bmatrix} + \begin{bmatrix} \frac{D + \Delta D}{L} \\ 0 \end{bmatrix} V_s \tag{3.40}$$

subtracting equation 3.39 from equation 3.40

$$\begin{bmatrix} \Delta\dot{i_L} \\ \Delta\dot{V_o} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \Delta i_L \\ \Delta V_o \end{bmatrix} + \begin{bmatrix} \frac{\Delta D}{L} \\ 0 \end{bmatrix} V_{in} \tag{3.41}$$

To obtain the transfer function of ratio of output voltage to duty cycle, take the Laplace transform of equation 3.39

$$s \begin{bmatrix} I_L(s) \\ V_o(s) \end{bmatrix} - \begin{bmatrix} i_L(0) \\ V_o(0) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L(s) \\ V_o(s) \end{bmatrix} + \begin{bmatrix} \frac{D(s)}{L} \\ 0 \end{bmatrix} V_{in} \tag{3.42}$$

Assuming initial conditions zero and rearrange the terms to get

$$\begin{bmatrix} I_L(s) \\ V_o(s) \end{bmatrix} = \begin{bmatrix} s & \frac{1}{L} \\ -\frac{1}{C} & s + \frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \frac{D(s)}{L} \\ 0 \end{bmatrix} V_{in} \tag{3.43}$$

Taking the inverse of the matrix in equation 3.43, following equation is obtained.

$$\begin{bmatrix} I_L(s) \\ V_o(s) \end{bmatrix} = \frac{1}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \begin{bmatrix} s + \frac{1}{RC} & -\frac{1}{L} \\ \frac{1}{C} & s \end{bmatrix} \begin{bmatrix} \frac{D(s)}{L} \\ 0 \end{bmatrix} V_{in} \tag{3.44}$$

In a closed loop system, duty cycle D is varied in order to maintain the output constant. Thus the transfer function is obtained as follows

$$\frac{V_o(s)}{D(s)} = \frac{V_{in}}{1 + s\frac{L}{R} + s^2LC} \tag{3.45}$$

To obtain the transfer function of ratio of output voltage to input voltage rearranging the terms of above equation following equation is obtained.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{D}{1 + s\frac{L}{R} + s^2LC} \tag{3.46}$$

Equation 3.46 represents the damped second order low pass filter response.

3.4 Buck converter Design

The design of a buck converter involves the calculation of values of the inductor and capacitor.The parameters of buck converter are obtained from the equations derived in section 3.2.Rearranging the terms of equation 3.6 the expression of inductor is obtained as

$$L = \frac{V_{in}TD(1-D)}{\Delta i_L} \tag{3.47}$$

where T is the time period and Δi_L is the peak to peak ripple current of the inductor. Similarly, equation 3.15 gives the expression for the capacitance

$$C = \frac{\Delta i_L}{8 f_s \Delta V_o} \tag{3.48}$$

where ΔV_o is the peak to peak output voltage ripple.

A set of desired specifications and the designed values of buck converter are tabulated in table 1

Simulation is performed using Matlab Simulink for the buck converter. The open loop buck converter model is shown in figure 3.5. A PWM signal is given at the gate source of the MOSFET and the output is observed across the load resistance.

Table 3.1: Buck Converter Parameters

Parameters	Design Value
Input Voltage V_{in}	24V
Output VoltageV_o	12V
Output Current I_o	2A
Max.Power Pmax	24W
Switching Frequency fs	25kHz
Inductor Current ripple Δi_L	10%
Output Voltage rippleΔV_o	0.1%
Inductor L	2.4mH
Capacitor C	450uF
Load Resistance R	6 Ohms

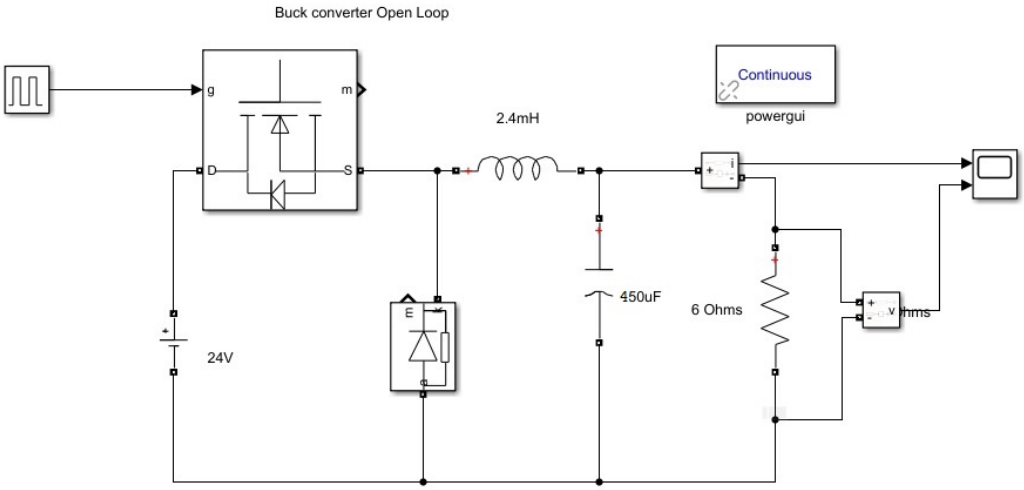

Figure 3.5: Open Loop Buck converter model

The output voltage and the load current is shown in figure 3.6. It can be seen that in a open loop configuration, the output voltage is 11.7V which is less than desired value of 12V. The output current is 1.9A less than the desired value of 2A. Hence compensation with a controller is required to obtain a regulated output.

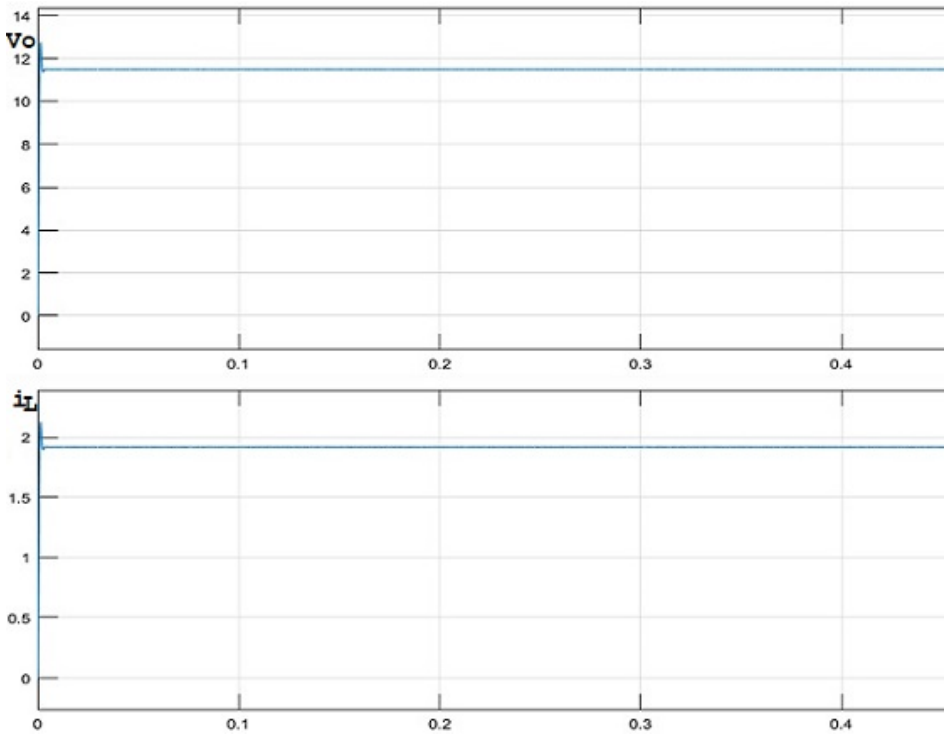

Figure 3.6: Open Loop Buck converter Simulation

3.5 Compensation for a Buck converter

A compensation technique is used to regulate the output voltage of the buck converter using a feedback loop.The output voltage depends on switching duty cycle and the input voltage. The duty cycle is adjusted accordingly so as to achieve the desired output voltage with a high accuracy, regardless of variations in input voltage V_{in} or the load current I_o or variations in component values.

A block diagram of the buck converter with a feedback loop is shown in figure 3.7.

The output voltage V_o is measured with a sensor having a gain $H(s)$. The sensor circuit usually consists of a voltage divider using precision resistors. The sensor output $H(s)V_0$ is compared with the reference input voltage $V_{ref}(s)$. The difference between the $V_{ref}(s)$ and $H(s)V_0$ is the error voltage. The objective is to make this error voltage $V_e(s)$ minimum. The compensator with a gain of $G_c(s)$ is added in the forward loop. The output voltage is the product of error voltage, compensator gain, pulse width modulator gain and the converter power stage gain.

The converter is assumed in a continuous conduction mode and duty cycle is taken as the controlled variable. The output voltage is dependent on the changes in the input voltage

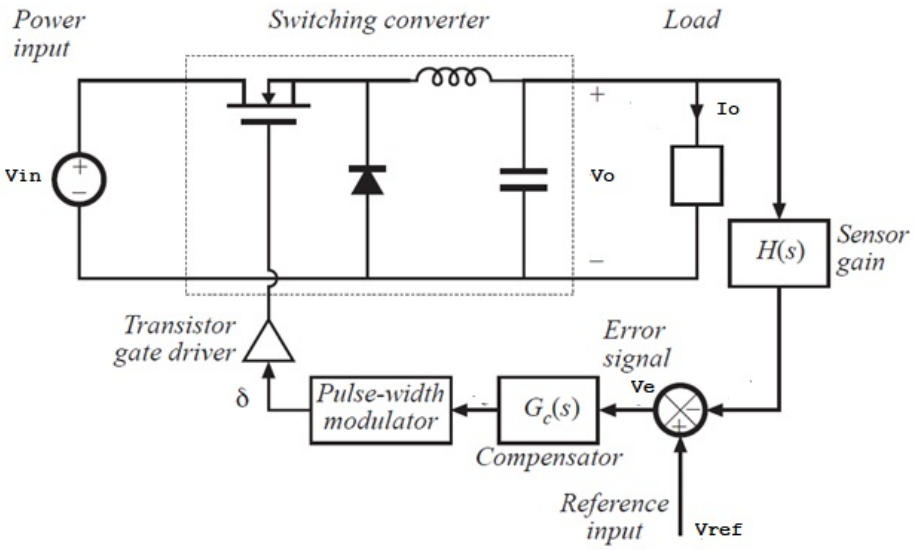

Figure 3.7: Buck Converter closed loop configuration[1]

and the switch is assumed ideal thereby neglecting the non idealities due to its switching. Control loop is with $H(s)$ as sensor gain, $G_c(s)$ is the transfer function of the compensator and 1/V_m is the gain of the pulse width modulator .

The loop gain T(s) is given by

$$T(s) = H(s)G_c(s)G_{vd}(s)/V_m \tag{3.49}$$

where G_{vd} is given by equation 3.46. To analyse the system, following assumptions are made.

1. The transfer function of disturbance to the output is multiplied by the factor 1/(1+T(s)). If the loop gain T(s) is large in magnitude, the influence of the disturbance on the output voltage is small. Hence the loop gain T(s) is a measure of effectiveness of the feedback loop.

2. Other important parameter of feedback systems is stability. The feedback loop can cause a well behaved circuit to exhibit ringing and overshoot along with oscillations. The phase margin criterion is used to assess the stability. If the phase margin of the loop gain T(s) is positive then the system is stable. Also increasing the phase margin will lead to a better system transients response with less overshoot.

Substituting the design values in the equation 3.46, open loop transfer function of the

buck converter is obtained as

$$G_{vd}(s) = \frac{V_o(s)}{D(s)} = \frac{24}{1 + 0.0004s + 1.08X10^{-6}s^2} \tag{3.50}$$

The loop transfer function is calculated as given in equation 3.49.The sensor gain $H(s)$ is assumed to be 1/3 and $V_m = 4$. Assuming $G_c(s) = 1$ which is the uncompensated system and substituting the values the loop gain is obtained as

$$T_o(s) = \frac{2}{1 + 0.0004s + 1.08X10^{-6}s^2} \tag{3.51}$$

where T_o is the uncompensated loop transfer function.

Corner frequency $f_c = w_o/2\pi = 1/2\pi\sqrt{(LC)} = 153Hz$ = 961.3rad/s

Quality factor $Q_o = R\sqrt{(C/L)} = 2.598 = 8.29dB$

Frequency domain analysis is carried out using Bode plots [29]. The transfer function is simulated in Matlab to obtain the plot. A Bode plot of the transfer function T(s) is plotted in Matlab and is shown in figure 3.8. The phase margin is obtained as 19.1^o at a gain cross over frequency of 1.64krad/sec.

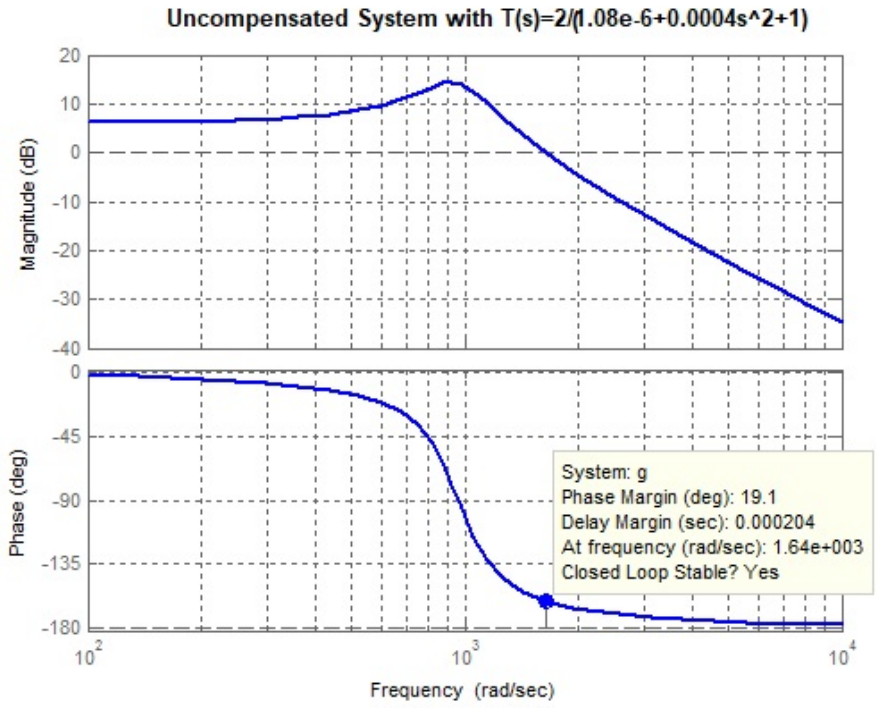

Figure 3.8: Bode Plot for uncompensated buck converter

Figure 3.9 shows the simulation of the buck converter using Matlab simulink. The closed loop configuration is used without any compensation. The output waveform for change in

input voltage is shown in figure 3.10. It is a distorted output and the closed loop system is required to be compensated. PI, Lead, Lead with PI and PID compensators are selected to analyse the buck converter performance in frequency and time domain.

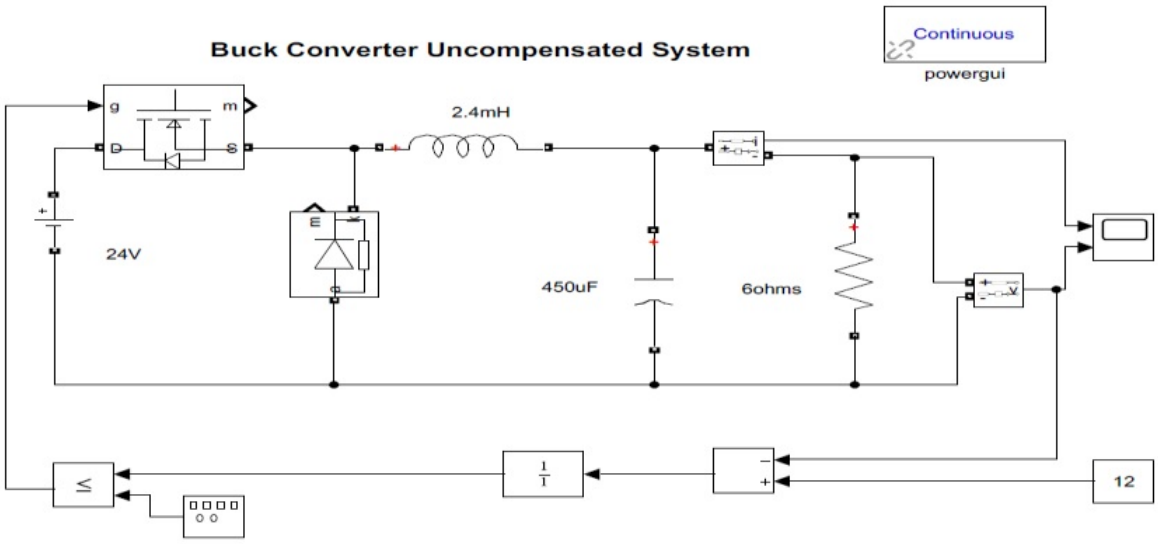

Figure 3.9: Matlab Simulation of an Uncompensated system

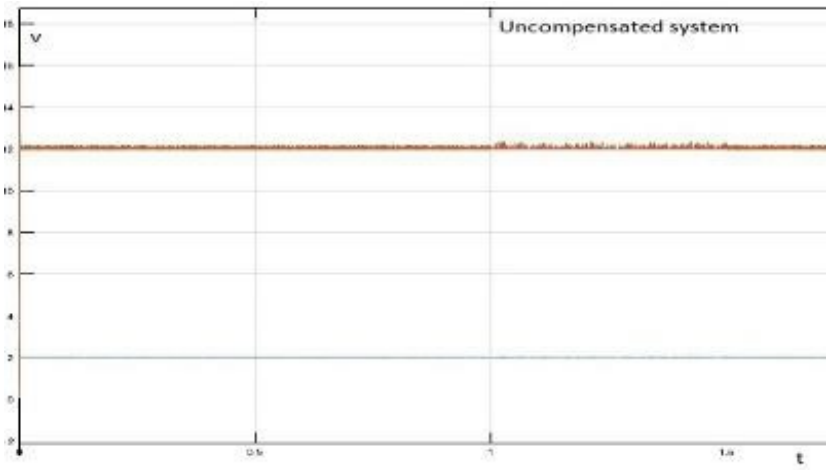

Figure 3.10: Uncompensated simulink waveform

The steps used to analyse the response are described below

1. The compensator transfer function $G_c(s)$ is designed by placing its zeros and poles to improve the phase margin and the time domain response.

2. The loop gain of the buck converter $T_o(s)$ is calculated by the equation

$$T(s) = T_o(s)G_c(s) \tag{3.52}$$

3. Bode plot of $T(s)$ is plotted to obtain the frequency domain response. The Phase margin and gain cross over frequency is obtained from Bode plots

4. The simulink model is simulated with the compensator for changes in input voltage. The time domain response is analysed for overshoot, settling time and change in output voltage.

In the next section, the compensators are designed and tested to obtain the designed phase margin . The output voltage changes are observed for increase and decrease of the input voltage.

3.5.1 Proportional Integral (PI) Compensator

This type of compensator is used to increase the low frequency loop gain so that the output is regulated well for frequencies below the loop crossover frequency.

The transfer function of this compensator is given by

$$G_c(s) = G_{co}\frac{(1+\frac{s}{w_z})}{s} \tag{3.53}$$

The PI compensator has a high gain at low frequencies which falls at -20dB per decade and then levels out at zero frequency f_z. The phase is initially -90^0, which increases by a rate of 45^0 per decade starting at $f_z/10$ to a maximum of 0^0 at $10f_z$. The high gain at low frequencies eliminates steady state error to step input. The zero is placed at $f_z = f_o/10 = 15.3Hz$ Hence $w_z = 2\pi f_z = 96.132rad/s$.

The compensated loop gain T(s)=1.

The transfer function of this compensator is given by

$$T(s) = \frac{T_o G_{co}}{2\pi f_z} = 1 \tag{3.54}$$

Hence, G_{co} is given as

$$G_{co} = \frac{2\pi X 15.3}{2} = 48 \tag{3.55}$$

The transfer function of the compensator after substituting the values is then calculated as follows

$$G_c(s) = 48\frac{(1+\frac{s}{96.132})}{s} \tag{3.56}$$

The loop gain of the buck converter with PI compensator can be expressed as

$$T(s) = T_o G_{co} \frac{(1 + \frac{s}{w_z})}{s(1 + \frac{s}{Qw_0} + (\frac{s}{w_0})^2)} \tag{3.57}$$

By substituting the values in equation 3.57, the loop transfer function is obtained as follows

$$T(s) = 48 \frac{(1 + \frac{s}{96.132})}{s} \frac{2}{1 + 0.0004s + 1.08X10^{-6}s^2} \tag{3.58}$$

The Bode plot of loop gain with PI compensator is plotted using Matlab and is shown in figure 3.11

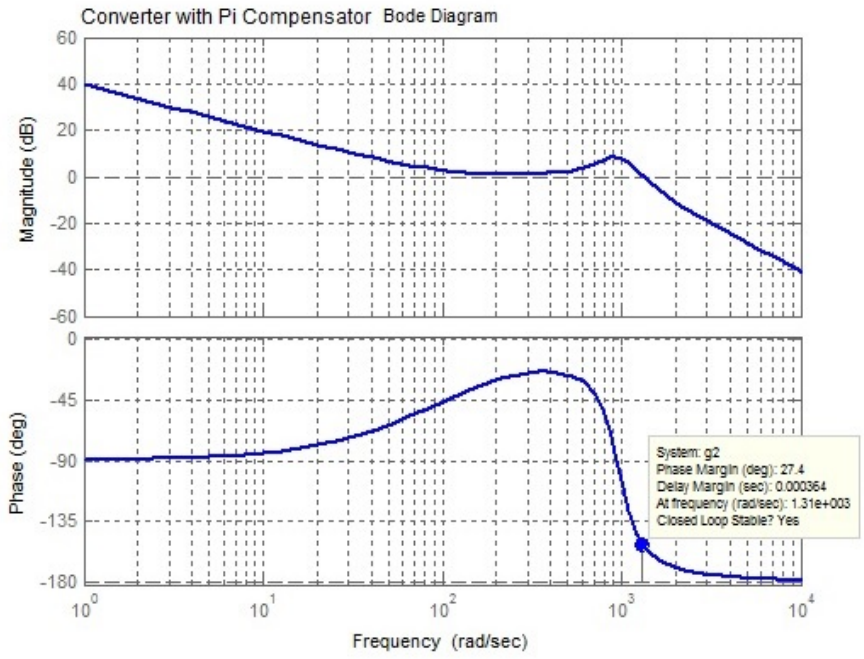

Figure 3.11: Bode plot of buck converter with PI compensation

From the plot, it is observed that the Phase Margin is 27.4^0 and gain cross over frequency w_{gc} is obtained as 1.31krad/s.

A Matlab Simulink Model is simulated using the PI controller. The controller block is simulated with the transfer function of the PI Controller. The model is as shown in figure 3.12.

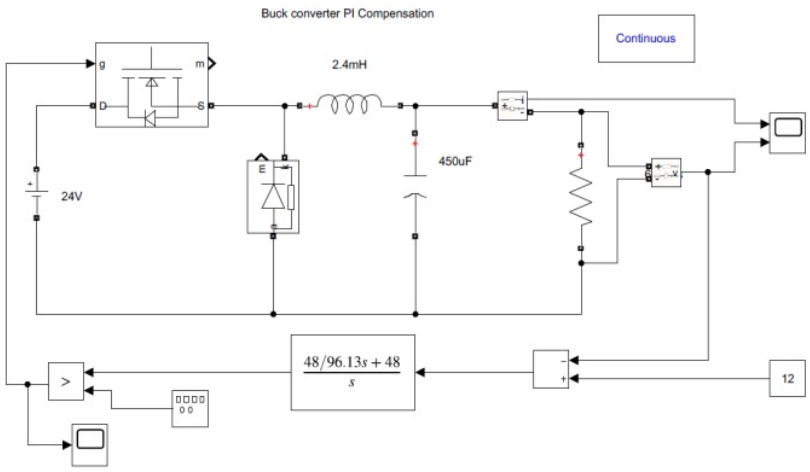

Figure 3.12: Buck Converter model with PI compensation

The model is simulated for changes in the input voltage. The input voltage is set to 24V and the output is observed. It is found that the regulated output of 12V is obtained as shown in figure 3.13. The input voltage is then set to 20V and the output is observed. The transient response and the steady state response is observed. Similarly the input is set to 28V and the output is observed. The overshoot is observed to be 2.11% and the settling time is 40msecs.

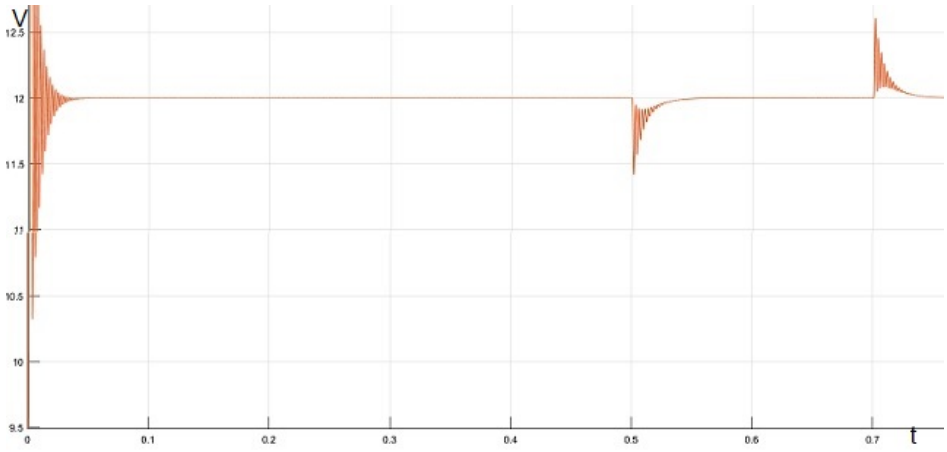

Figure 3.13: Buck Converter output for PI compensation

3.5.2 Lead Compensator

The performance of the buck converter is improved by using a lead compensator. The transfer function of this compensator is given by

$$G_c(s) = G_{co}\frac{(1+\frac{s}{w_z})}{(1+\frac{s}{w_p})} \tag{3.59}$$

where $w_z < w_p$. The zero is placed at lower frequency than the pole frequency. It provides a phase boost which is adjustable based on the pole and zero frequencies and a gain boost at higher frequencies giving a higher crossover frequency. Thus the phase margin of the converter can be improved. The design is carried out for a gain margin of $\phi_m = 52^0$ and a crossover frequency of $f_c = 5KHz$. The poles and zeros are calculated as follows

$$f_z = f_c\sqrt{(1-\phi_m/1+\phi_m)} = 1.72Khz$$
$$f_p = f_c\sqrt{(1+\phi_m/1-\phi_m)} = 14.5Khz$$
$$G_{co} = (5000/153)^2\sqrt{(1.72/14.5)(0.5)} = 184$$

The transfer function of the lead compensator can be written as follows by substituting the values in equation 3.59.

$$G_c(s) = 184\frac{(1+\frac{s}{2\pi X1.72X10^3})}{(1+\frac{s}{2\pi X14.5X10^3})} \tag{3.60}$$

The loop gain of the buck converter with lead compensator can be expressed as

$$T(s) = T_oG_{co}\frac{(1+\frac{s}{w_z})}{(1+\frac{s}{w_p})(1+\frac{s}{Qw_0}+(\frac{s}{w_0})^2)} \tag{3.61}$$

Substituting the values in equation 3.61, loop gain is obtained as follows

$$T(s) = 184\frac{(1+\frac{s}{10807.1})}{(1+\frac{s}{91106.2})}\frac{2}{1+0.0004s+1.08X10^{-6}s^2} \tag{3.62}$$

The Bode plot of the loop gain with Lead compensator is plotted and shown in figure 3.14. From the Bode plot, the phase margin is 52.7^o and gain cross over frequency w_{gc} is 31.5 krad/s.

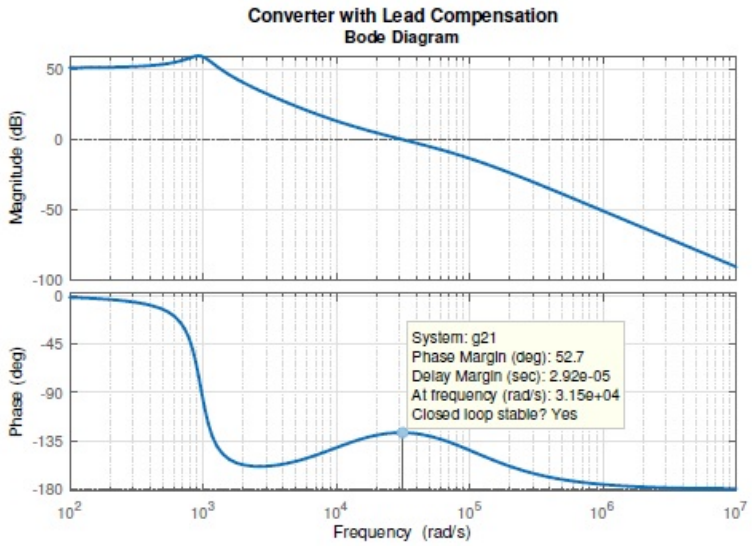

Figure 3.14: Bode plot of buck converter with lead compensation

The Matlab Simulink Model is designed with the Lead compensator transfer function as shown in figure 3.15. The model is simulated with changes in the input voltage and the output is plotted as shown in figure 3.16. The time required for the output to settle to 12V is observed. It is observed that there is very less overshoot of 0.013% and hence the transient response of the lead converter is good but has a large settling time and hence its steady state response is poor.

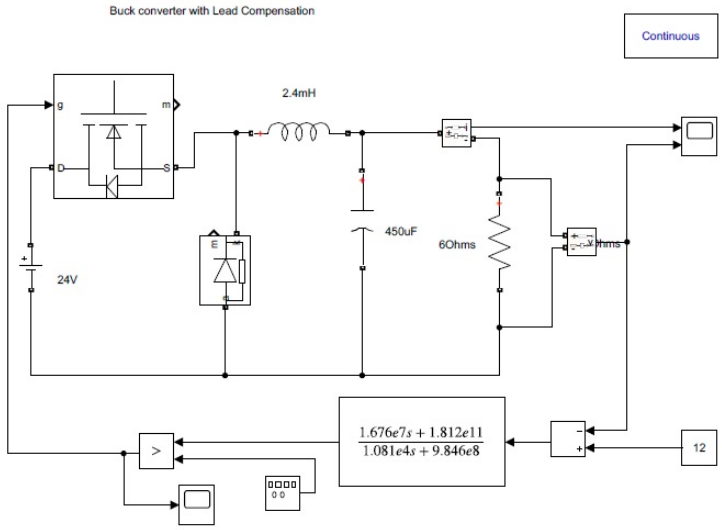

Figure 3.15: Buck Converter with Lead compensation model

Figure 3.16: Buck Converter Output with Lead compensation model

3.5.3 Combined PI and Lead Compensator

This compensator combines the properties of both PI and lead compensators. PI had good steady state response but not very good transient characteristics whereas lead has a very good transient response but a bad steady state characteristics. Thus PI with lead compensator combines the responses to gives a better transient and steady state response. The transfer

function of this compensator is given by equation 3.63

$$G_c(s) = G_{co}\frac{(1+\frac{s}{w_{z1}})(1+\frac{s}{w_{z2}})}{s(1+\frac{s}{w_p})} \tag{3.63}$$

To design this compensator, it is needed to know the placement of the two zeros and the pole. Here, w_{z2} is the zero introduced by the lead compensator and hence w_{z2}<w_p. It is assumed that the two compensator portions do not interact. To distinguish the effects of lead and PI compensation, it is assumed that w_{z1}<w_{z2}. To design the PI compensator at low frequencies and Lead compensator at high frequencies, the zeros and poles are chosen as follows

$f_{z1} = 50, f_{z2} = 132, f_p = 105KHz.$

The compensator is designed for a gain margin of $\phi_m = 52^0$ and a crossover frequency of $f_c = 5kHz$. Since a large gain at low frequencies is better, we design the combined compensator to have a gain factor $G_{co}T_o$ to be 1000.

The loop gain of the buck converter with Lead compensator can be expressed as

$$T(s) = T_oG_{co}\frac{(1+\frac{s}{w_{z1}})(1+\frac{s}{w_{z2}})}{s(1+\frac{s}{w_p})(1+\frac{s}{Qw_0}+(\frac{s}{w_0})^2)} \tag{3.64}$$

Substituting the values of the compensator transfer function in the loop transfer function a combined transfer function is obtained in equation 3.64

$$T(s) = 1000\frac{(1+\frac{s}{314})(1+\frac{s}{31415.9})}{s(1+\frac{s}{314159.27})(1+0.0004s+1.08X10^{-6}s^2)} \tag{3.65}$$

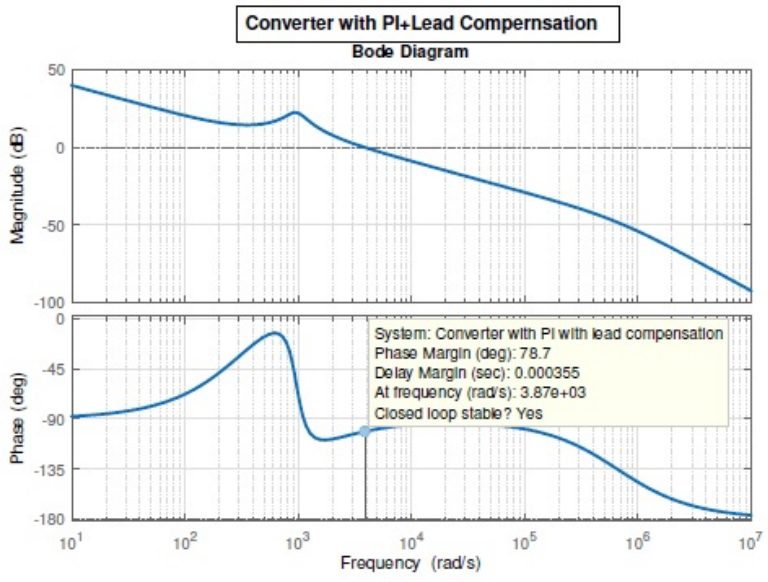

Figure 3.17: Bode plot of buck converter with PI and Lead compensation

The Bode plot of loop gain of the above compensator is plotted and shown in figure 3.17. From the Bode plot it is observed that the Phase Margin is 78.8 and gain cross over frequency w_{gc} is 3.9krad/s The Matlab Simulink model is simulated with the transfer function block of PI and lead compensator as shown in figure 3.18. The output of the converter with changes in input is shown in figure 3.19.It can be seen that PI and lead compensator gives a better transient and steady state response as compared with lead compensator alone. The overshoot is observed to be 0.33% and the settling time is 15msecs.

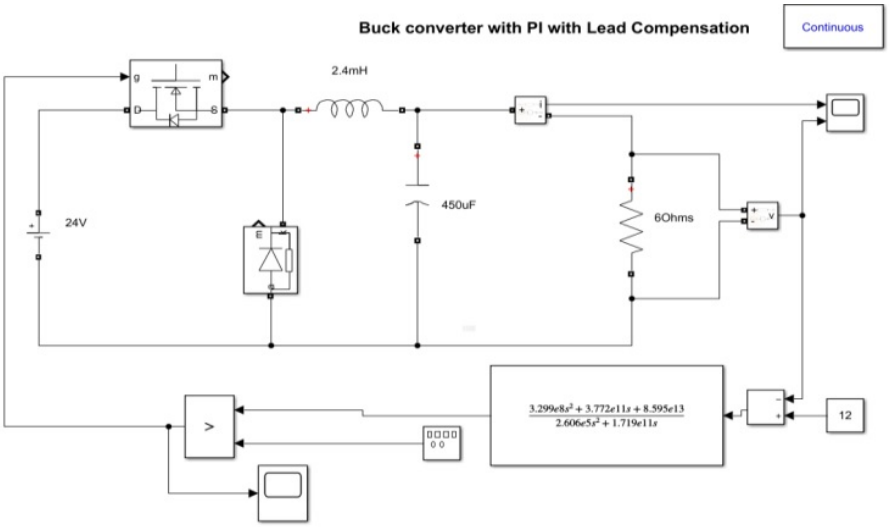

Figure 3.18: Buck Converter with PI and lead compensation model

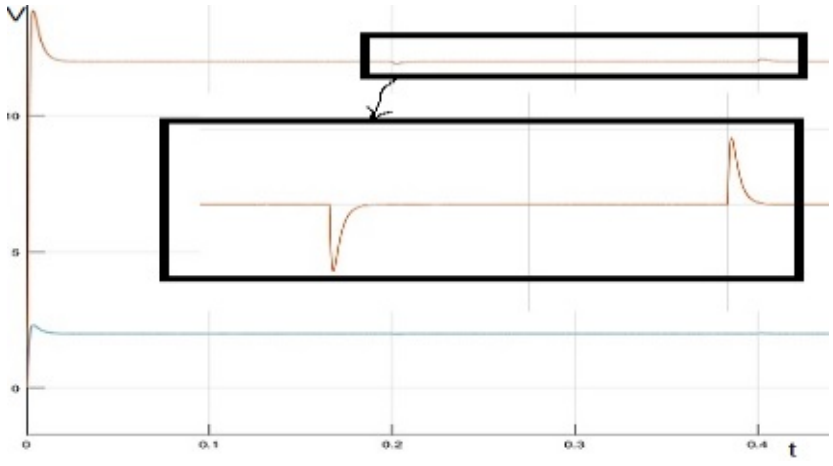

Figure 3.19: Buck Converter Output with PI with lead compensator

3.5.4 PID Compensator

PID compensator combines the advantages of PI and PD compensation. At low frequencies, the compensator integrates the error signal. Thus we have a large low frequency loop gain and hence accurate regulation of the low frequency components of the output voltage. At high frequency, it gives a phase lead into the loop gain. Thus the phase margin can be improved. The transfer function of this compensator is given by equation 3.66

$$G_c(s) = G_{co}\frac{(1+\frac{s}{w_z})(1+\frac{w_L}{s})}{(1+\frac{s}{w_p})} \tag{3.66}$$

The inverted zero at f_L functions as a PI compensator while the zero at f_z adds a phase lead in the vicinity of the crossover frequency for a PD compensator. The pole f_p is present to cause gain roll off at high frequencies and to prevent switching ripple in the pulse width modulator. To derive the PID compensation, an inverted zero is added to the lead Compensation transfer function equation . The design of cross over frequency f_c is 5khz and the phase margin is $\phi_m = 52^0$. The inverted zero f_L is chosen to be one tenth of the crossover frequency so that it does not significantly degrade the phase margin. The value is selected as f_L = 300 Hz to improve the low frequency regulation of the output voltage.

By keeping the other values same as Lead compensator, the transfer function of PID compensator is realised as follows

$$G_c(s) = 184\frac{(1+\frac{s}{2\pi X1.72X10^3})(1+\frac{2\pi X300}{s})}{(1+\frac{s}{2\pi X14.5X10^3})} \tag{3.67}$$

The loop gain of the buck converter with PID compensator can be expressed as

$$T(s) = T_o\, G_{co}\frac{(1+\frac{s}{w_z})(1+\frac{w_L}{s})}{(1+\frac{s}{w_p})(1+\frac{s}{Qw_0}+(\frac{s}{w_0})^2)} \tag{3.68}$$

Substituting the values of the compensator transfer function in the loop transfer function, the combined transfer function is obtained.

$$T(s) = 368\frac{(1+\frac{s}{10807.1})(1+\frac{1884}{s})}{(1+\frac{s}{91106.2})(1+0.0004s+1.08X10^{-6}s^2)} \tag{3.69}$$

The Bode plot of loop gain of the above compensator is plotted and shown in figure 3.20.From the Bode plot it is observed that the phase Margin is 49.2^0 and gain cross over frequency w_{gc}=31.5 krad/s = 5kHz, thus validating the design parameters.

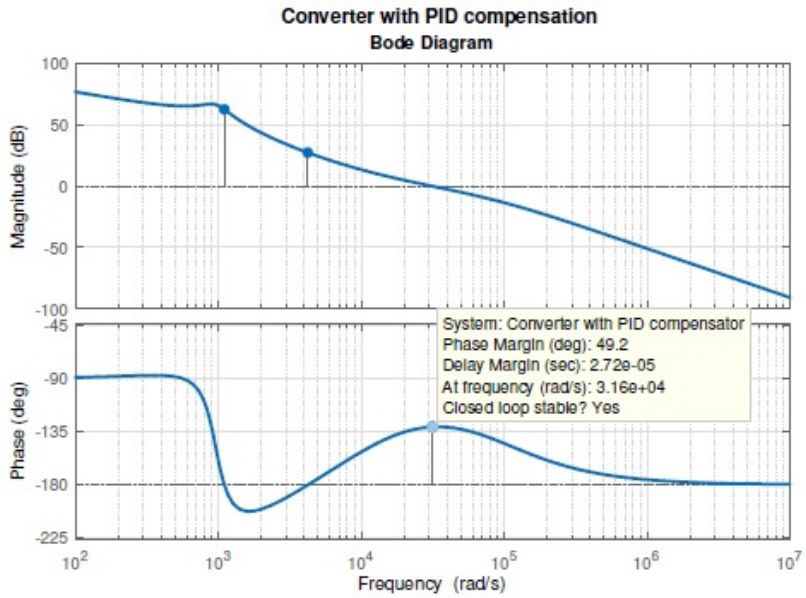

Figure 3.20: Bode plot of buck converter with PID compensation

The Matlab Simulink model is simulated with the transfer function block of PID compensator as shown in figure3.21. The output of the converter with changes in input is shown in figure 3.22

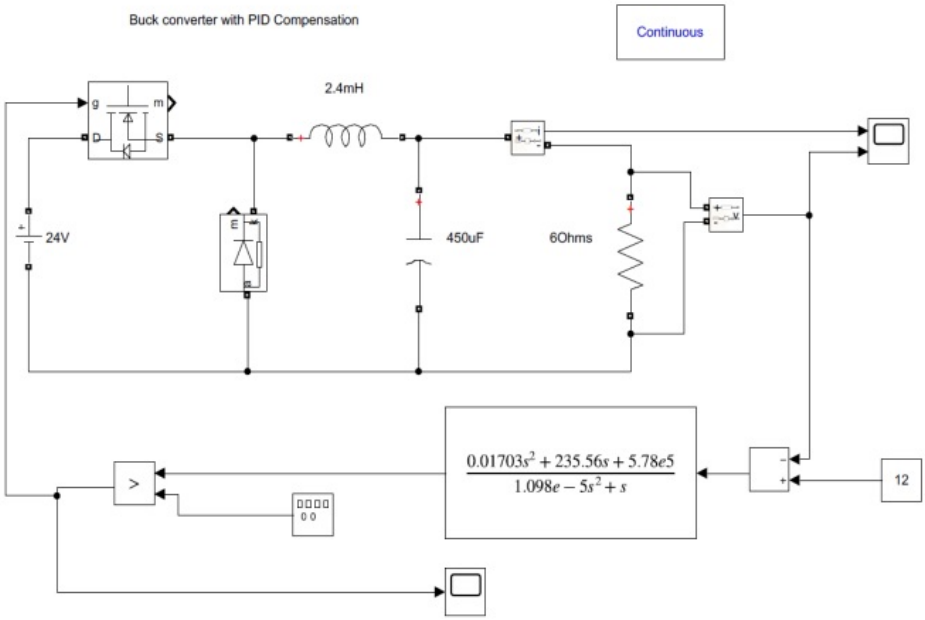

Figure 3.21: Buck Converter PID compensation model

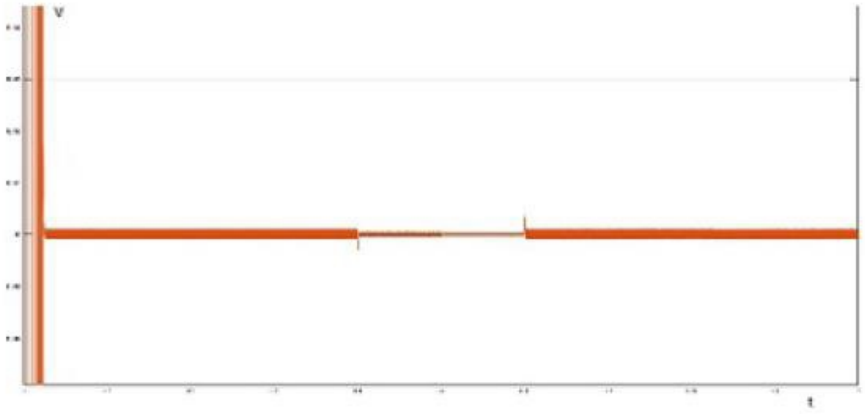

Figure 3.22: Buck Converter Output with PID compensator

The output shows a faster transient and steady state response as compared to the earlier compensators. The overshoot is observed to be 0.03% and the settling time is 1.5msecs.

3.5.5 Results

A comparative study of the four compensators for a DC-DC Buck converter using PI, lead, PI and lead and PID controllers was undertaken for frequency domain analysis using Matlab. Bode plots were plotted for individual compensators and then used with the converter to analyse the loop gain. A combined Bode plot of all four compensators is as shown in figure 3.23.

Results of Frequency Domain analysis of the phase margin and the gain crossover frequency is tabulated in Table 3.2

Table 3.2: Frequency Domain Analysis for buck converter

Type of compensators	Phase Margin in degrees	Gain cross over frequency krad/s
PI	27.4	1.31
Lead	52.7	31.5
Pi with Lead	78.7	3.87
PID	49.2	31.6

The time domain responses of the buck converter with various compensators are calcu-

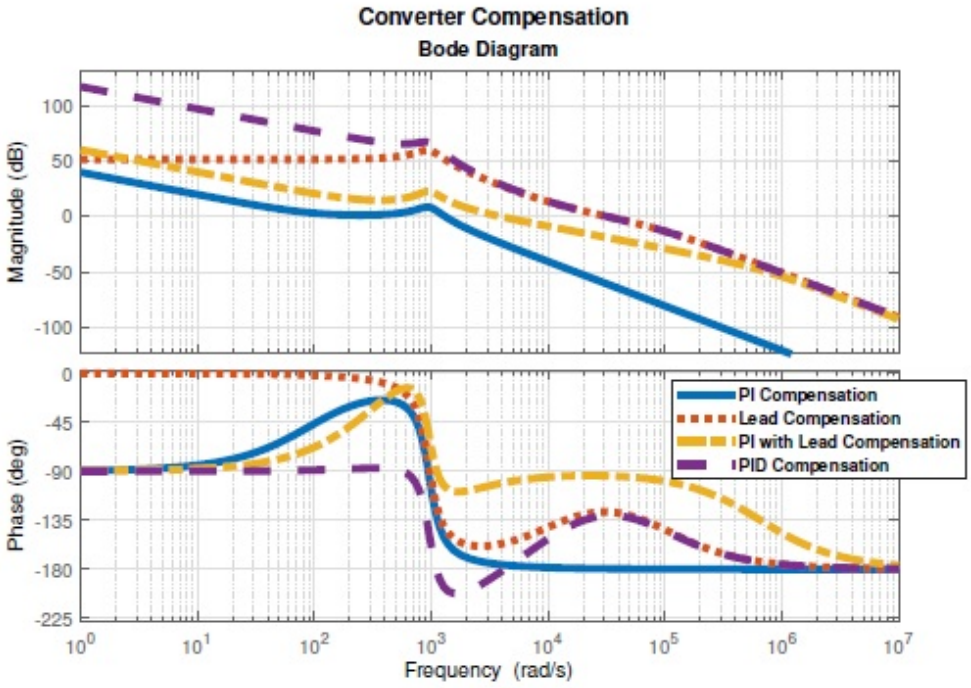

Figure 3.23: Combined Bode Plot for buck converter with the compensators

lated from the output response of the Matlab Simulink model. The responses of all four compensators are shown in figure 3.24

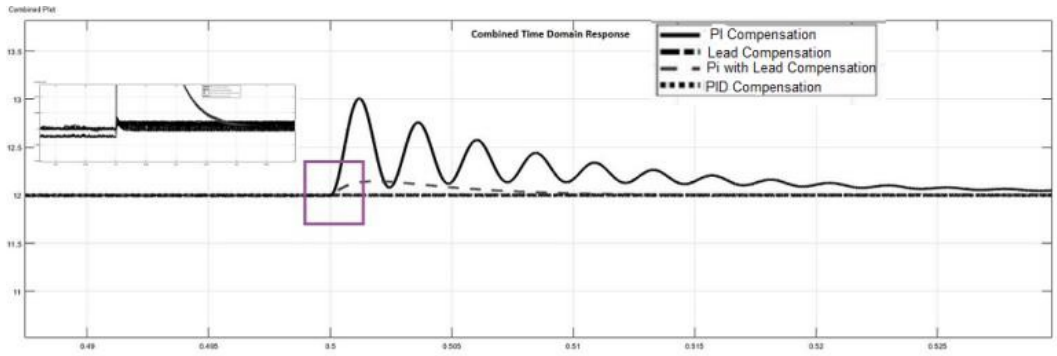

Figure 3.24: Combined time domain response of buck converter with the compensators

Transient and steady state characteristic are observed for the output of compensators. The percentage overshoot and settling time is found out. The peak voltage variation ΔV_o is also calculated. The comparative results are presented in Table 3.3

Table 3.3: Time Domain Analysis for buck converter

Type of compensators	overshoot in $\%$	Settling time in msecs	ΔV_o mV
PI	2.11	40	508
Lead	0.013	large	3
PI with Lead	0.33	15	80
PID	0.03	1.5	7

From the results, it is found out that the PID compensator gives a high phase margin of 49.2^o. Settling time of 1.5msec is achieved for PID which is the fastest of all compensators. The PI with lead compensator has the highest phase margin but the gain crossover frequency is poor. Lead compensator is also giving a high phase margin as per design but the time domain response is very slow since it has a high settling time. PI control is the widely used control and hence it is decided to implement PI and PID compensators for the buck converter in hardware.

3.6 PI Controller design using stability boundary locus method

This section explains the design of an analog PI controller. The PI controller constants are required to be tuned in order to achieve the desired specifications. The most common method used in industry is Ziegler-Nichols method. Typically, these rules result in aggressive control performance. The design criterion for the Ziegler-Nichols tuning rules is a maximal step overshoot of 25%.

Since the uncompensated buck converter has an infinite gain margin and phase margin is very less, the objective is to design the buck converter for a desired phase margin of 45^0. PI controller constants are obtained using stability boundary locus method [33]. The method is very useful in designing the controller for a desired gain and phase margin. The PI controller has a transfer function is written in the form

$$G_c(s) = k_p + \frac{k_i}{s} \tag{3.70}$$

where k_p and $k_i$are the parameters of the PI controller.

The uncompensated buck converter has a transfer function of the type

$$T(s) = \frac{b_0}{a_2 s^2 + a_1 s + a_0} \tag{3.71}$$

In the implementation of the closed loop system, the buck converter is interfaced with the FPGA board. The FPGA output is a PWM output which will switch the MOSFET. The loop gain of the transfer function will be 4.8 considering the voltage divider circuit. The overall block diagram is as shown in the figure 3.25.

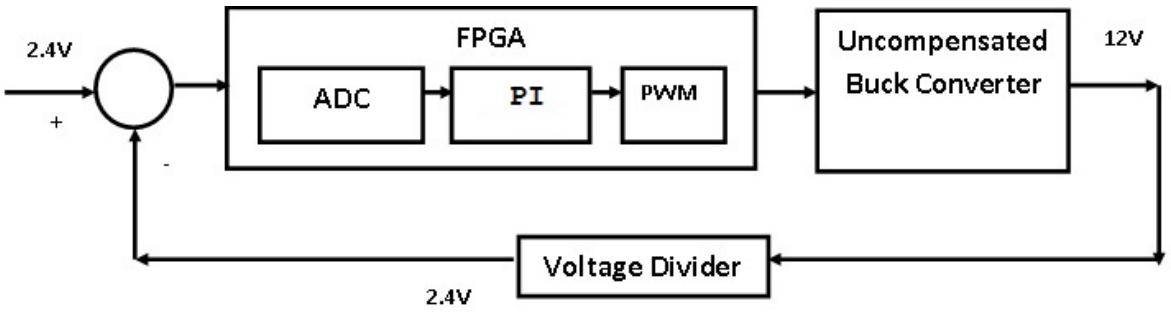

Figure 3.25: Implementation of the system

Let the desired phase margin be ϕ in degree. To satisfy this phase margin, the closed loop transfer function of the converter will have a characteristic equation of the form

$$\Delta(s) = 1 + e^{-j\phi} G_c(s) T_s = 0 \tag{3.72}$$

Substituting the values of equation 3.70 and 3.71 in equation 3.72

$$\Delta(s) = 1 + (cos\phi - jsin\phi)(k_p + \frac{k_i}{s})(\frac{b_0}{a_2 s^2 + a_1 s + a_0}) = 0 \tag{3.73}$$

Substituting s=jω, simplifying and putting

$A_1 = \omega b_0 sin\phi$,$A_2 = b_0 cos\phi$, $A_3 = \omega^2 a_1$,

$A_4 = \omega b_0 cos\phi$, $A_5 = -b_0 sin\phi$, $A_6 = \omega^3 a_2 - \omega a_0$,

the equation becomes

$$(k_p A_1 + k_i A_2) + j(k_p A_4 + k_i A_5) = A_3 + jA_6 \tag{3.74}$$

Equating real and imaginary parts of equation (38) and solving the resulting equations for $k_p$and k_i,we get

$$k_p = \frac{A_3 A_5 - A_6 A_2}{A_1 A_5 - A_4 A_2} \tag{3.75}$$

Substituting the values, k_p is obtained as follows

$$k_p = \frac{-b_0 sin\phi\omega a_1 - \omega^2 a_2 b_0 cos\phi + a_0 b_0 cos\phi}{-b_0^2} \tag{3.76}$$

Similarly,

$$k_i = \frac{A_3 A_4 - A_6 A_1}{A_2 A_4 - A_5 A_1} \tag{3.77}$$

$$k_i = \frac{\omega(a_2 b_0 sin\phi\omega^2 - a_1 b_0 cos\phi\omega - a_0 b_0 sin\phi)}{-b_0^2} \tag{3.78}$$

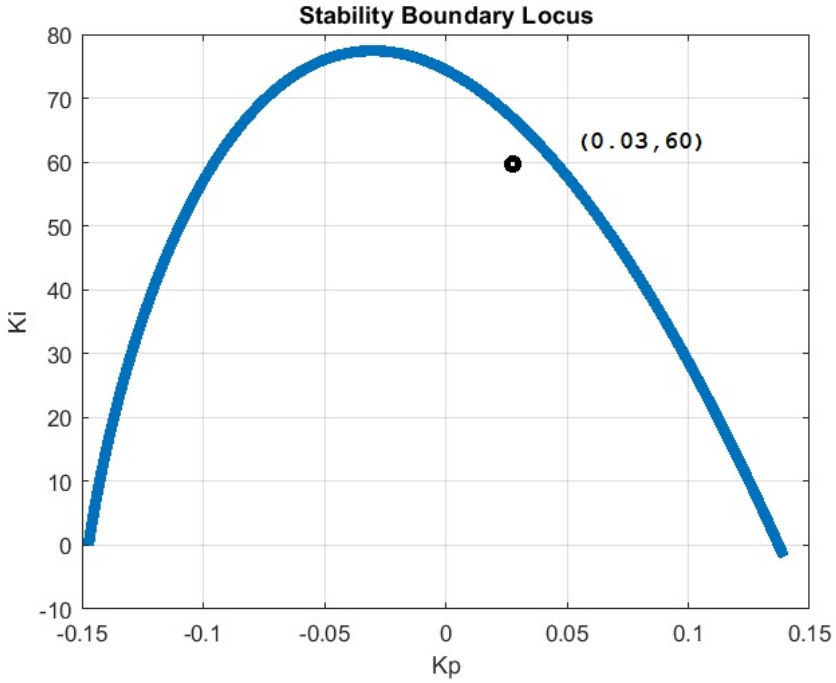

Figure 3.26: Stability Boundary Locus

Equation 3.76 and equation 3.78 give the boundary locus of the tuning parameters for a desired phase margin ϕ. Design of the PI controller is carried out for a phase margin of 45^0, and substituting the values of b_0 = 4.8, a_0 = 1 , a_1 = 0.0004 ,$a_2 = 1.08X10^{-6}$ for a range of frequencies, a stability boundary locus is obtained as shown in figure 3.26 .

From the stability boundary locus, different values of k_p and k_i are simulated for frequency domain analysis.

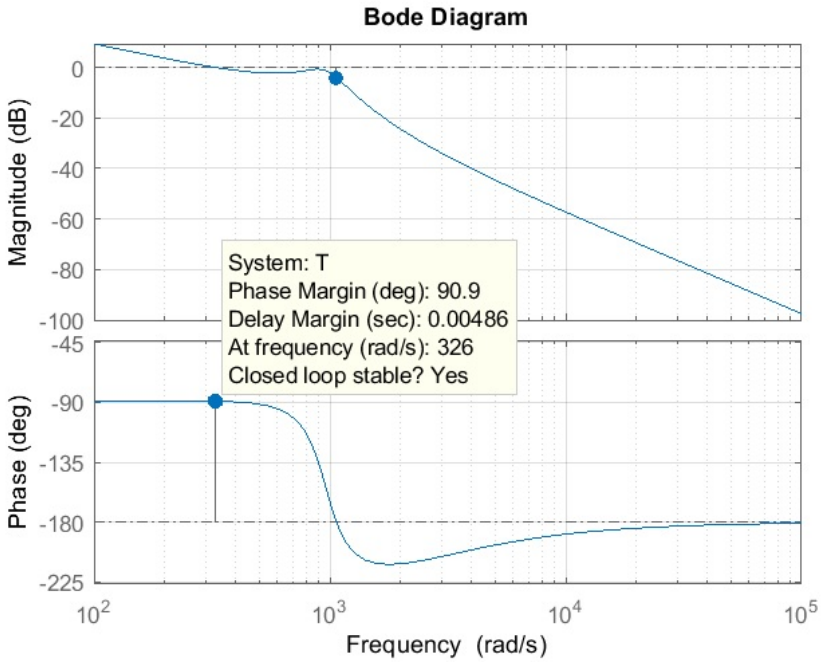

Figure 3.27: Frequency Response of Compensated Buck Converter using Stability boundary locus

The bode plot is shown in figure 3.27 It is found that a phase margin of 90.9^0 is obtained for $k_p = 0.03$ and $k_i = 60$. A high phase margin will improve the transient response. Also the 20db/decade slope at low frequencies will reduce the steady state error. Taking these as the tuned values, a closed loop simulation is obtained in Matlab Simulink.

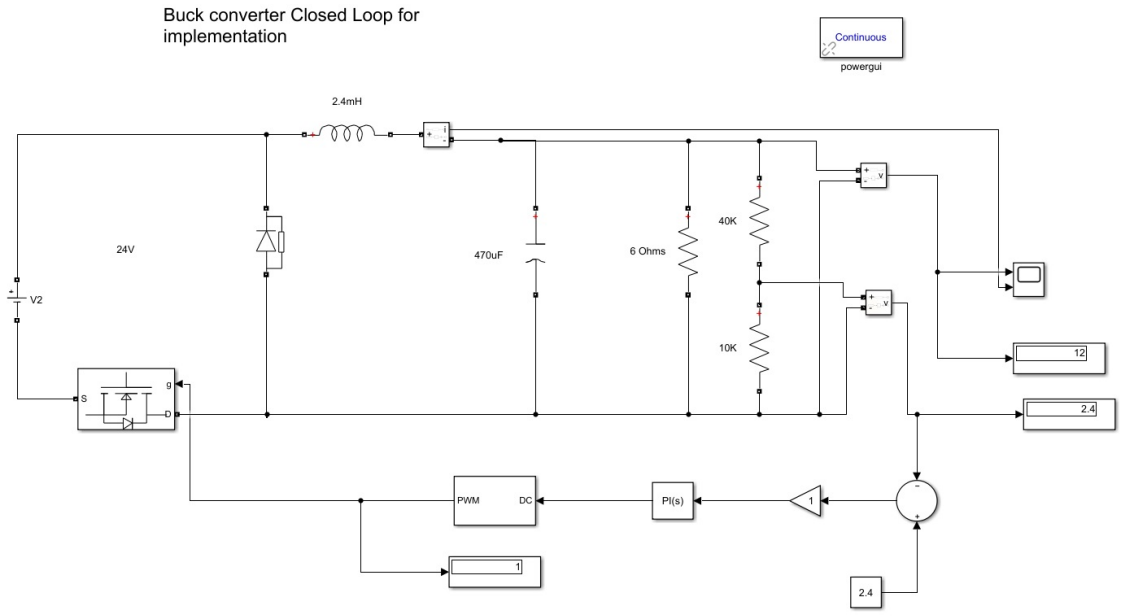

Figure 3.28: Closed loop Buck Converter Model with tuned PI values

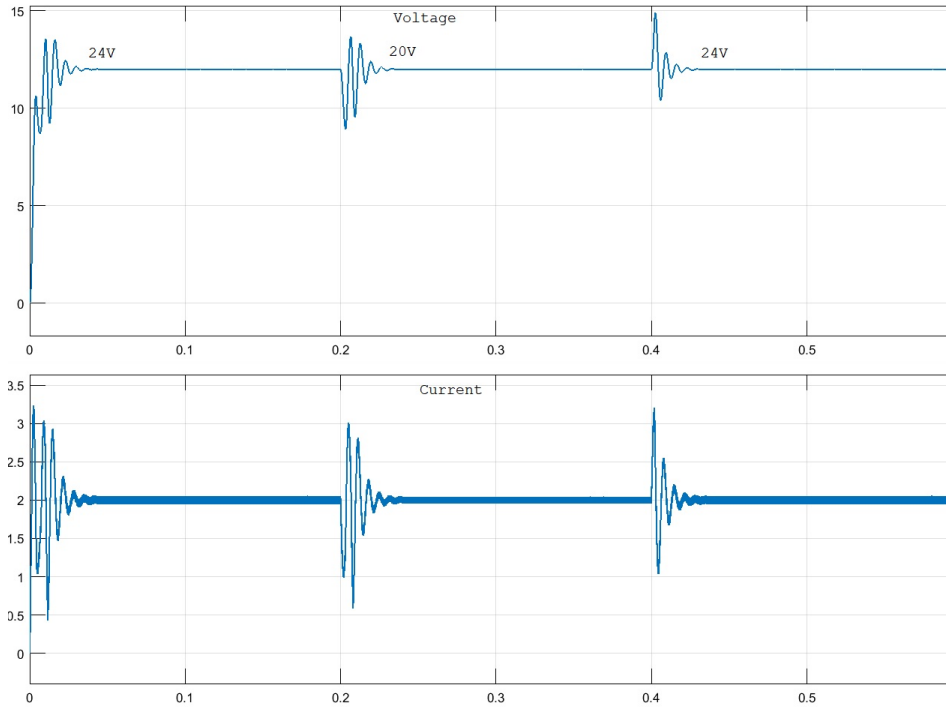

Figure 3.29: Closed loop Buck Converter Simulation with tuned PI values

A closed loop Simulink model is tested for changes in the input voltage. The switching mosfet is placed in the reverse path in order to have a common ground source. Figure 3.28 shows the model with the tuned values. The output is shown in figure 3.29. It can be see that the regulated output is achieved.

3.7 Component selection for buck converter

The buck converter is implemented using hardware components. The main components are inductor, diode, Power MOSFET, capacitor and load. The power supply is used to supply the necessary input.

1. **Inductor design**

   One of the challenging and most critical aspect in a power converter design is making of an inductor and to achieve desired inductance value. Major factors governing the proper design are

   - Core selection
   - Finding out number of turns

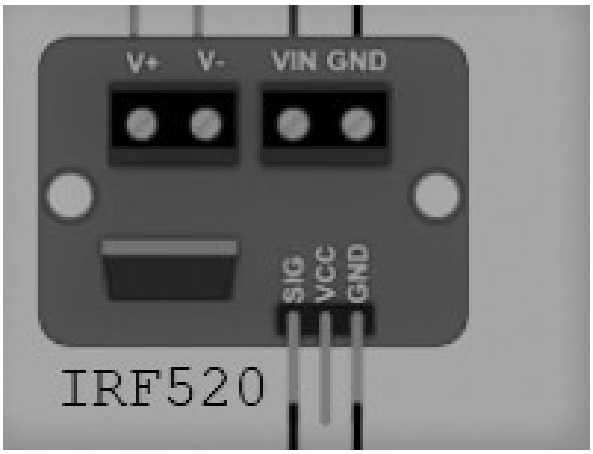

Figure 3.30: MOSFET IRF520 Board

- Wire gauge
- Number of parallel paths in one turn

Core is chosen from the available soft magnetic materials like ferrite, metglas, powdered iron etc. Unknown ferrite torrid core characteristics are the inductance factor A_L or the initial permeability of the core μ. These values are to be calculated. To estimate these values, the core is wound with some turns and inductance is measured by using an LCR meter. A ferrite core of 6mmX10mmX4mm was obtained. Winding wire gauge SWG 26 with d=0.457mm was wound for 8 turns. The inductance value was 169 μ H. With this value of permeability and the wire diameter, the number of turns for the required inductance was found out to be 27. The core was wound and the inductance value of 2.4mH was checked on the LCR meter.

2. **Power MOSFET**

   The Power mosfet is IRF520. A mosfet module is used as shown in figure 3.30. It is a n-channel enhancement mode mosfet with 100V, 10A current. The module has a gate and ground pin. The supply is connected to Vin and Gnd pins. The drain terminal is V^- and the V^+ is the positive of the supply. The source of the mosfet is having a connection to ground terminal of the supply. Thus the arrangement of mosfet in negative path is done. In addition a heat sink is connected to mosfet for heat dissipation.

3. **Power Diode**

The power diode plays a very important role when the MOSFET is switched off. The load current flows through the diode. Hence the power diode should have the switching frequency higher than the converter switching frequency. Schottky Diodes are used in switching converters due to its low forward voltage and fast turn on time. The diode selected is IN5822. It has 40V Repetitive peak reverse voltage and a 3A RMS forward voltage.

4. **Gate Driver**

   The driver circuit drives the MOSFET. It has a optocoupler at the input stage and the output stage is transistor stage to drive the switching device. The driver IC FOD3184 pin diagram is as shown in the figure 3.31

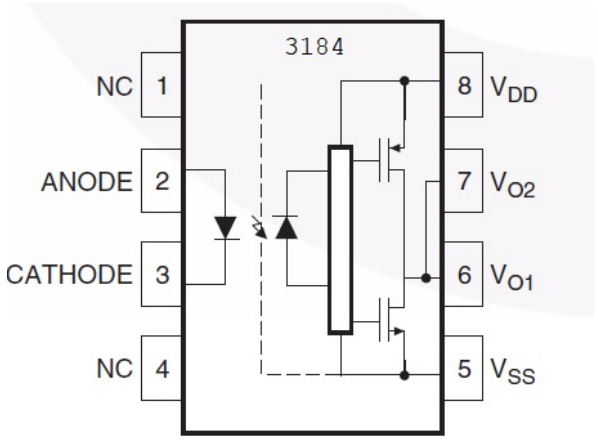

Figure 3.31: Mosfet driver

5. **Capacitor** A capacitor of 470μ F, 25V is chosen at the output stage.

6. **Resistors** A load of 10 ohm is taken at the output as load. Also the potential divider is connected to reduce the voltage to 2.4V

3.8 Hardware Implementation of a buck converter

The components are assembled and the interfacing of the FPGA board with the converter is performed. The schematic for the hardware implementation is as shown in figure 3.32. The buck converter is assembled with the designed inductor and the capacitor. The output of the buck converter is taken from a voltage divider and is given to FPGA as an analog input. The

digital comparator, PI controller and the PWM generator are synthesized and programmed on FPGA . The output of the FPGA is a PWM signal. The PWM output is given to the driver IC FOD3184 which is a optocoupler and driver. The output of the driver IC drives the gate of the MOSFET. Thus the closed loop control is achieved.

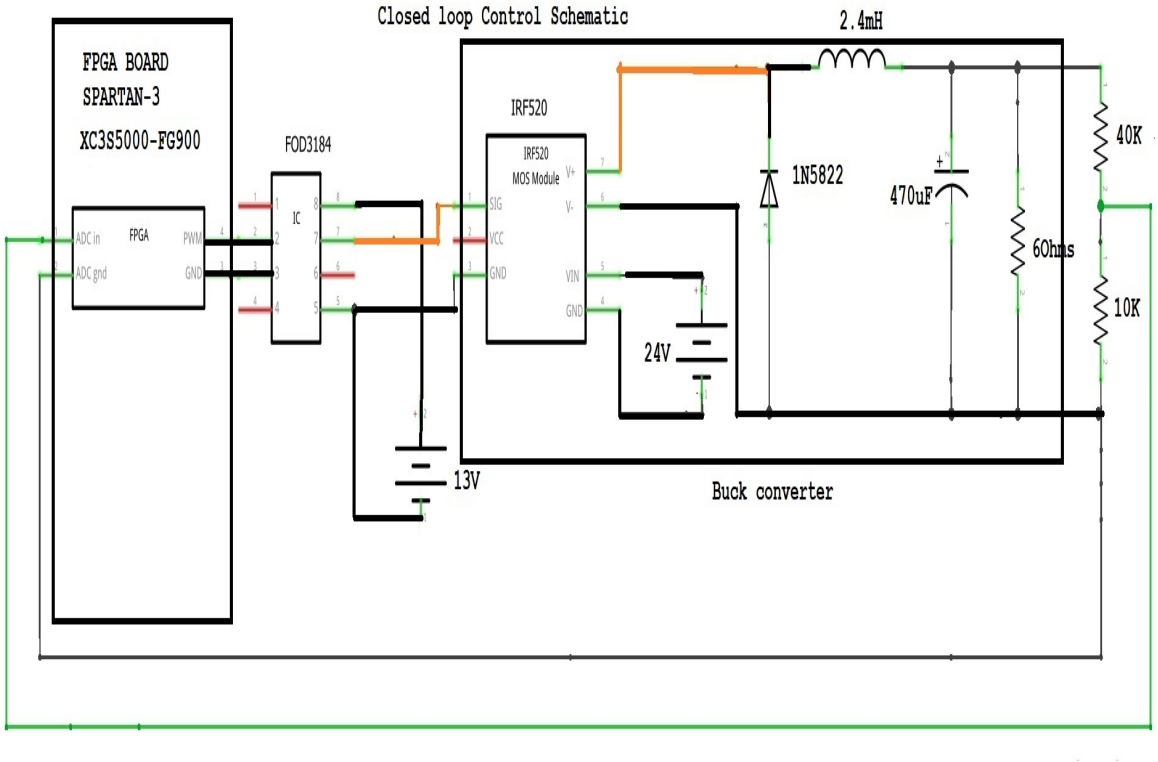

Figure 3.32: Hardware implementation schematic for a buck converter

3.9 Performance Evaluation of buck converter

DC-DC converter has a regulated output. The parameters that can have variations are input voltage and the load current. The output voltage V_o depends on the unregulated input voltage V_{in}, the load current I_o and the temperature T. The change in the output voltage of the switching converter is expressed as

$$\Delta V_o = \frac{\partial V_o}{\partial V_{in}}\Delta V_{in} + \frac{\partial V_o}{\partial I_o}\Delta I_o + \frac{\partial V_o}{\partial T}\Delta T \tag{3.79}$$

The three coefficients are defined as

1. Stability factor $S_v = \frac{\partial V_o}{\partial V_{in}}$ at $\Delta I_o = 0$ and $\Delta T = 0$

2. Output resistance R_o = $\frac{\partial V_o}{\partial I_o}$ at $\Delta V_{in} = 0$ and $\Delta T = 0$

3. Temperature Coefficient S_T = $\frac{\partial V_o}{\partial T}$ at $\Delta V_{in} = 0$ and $\Delta I_o = 0$

The stability factor, output resistance and the temperature coefficient give the output voltage change and hence voltage regulation is obtained. The ratio of the change in output voltage and the output voltage gives the voltage regulation of the converter. Evaluation is performed for stability and output resistance. Temperature change is ignored. The buck converter is analysed for its performance in open loop and closed loop configuration.

3.9.1 Open Loop Configuration

In the open loop configuration, a pulse width of varying duty cycles from 40% to 80% are generated using VHDL and downloaded on FPGA. The FPGA is programmed only for PWM output. The converter is given these pulses. The converter is subjected to constant input voltage keeping load current constant and observing the effect of varying duty cycle. Three sets of reading are taken and the variations are plotted.

1. Constant VoltageV_{in}=24V , Load Current I_l=0.25A

Table 3.4: Open Loop varying duty cycle 24V input

Sr.No	Duty Cycle%	Output Voltage V_o measured V	Output Voltage V_o calculated V	Load Ohms
1	40	9.4	9.6	32
2	50	12	12	45
3	60	14.7	14.4	50
4	70	16.9	16.8	64
5	80	18.6	19.2	75

2. Constant VoltageV_{in}=18V ,Load Current I_l=0.16A

Table 3.5: Open Loop varying duty cycle 18V input

Sr.No	Duty Cycle%	Output Voltage V_o measured V	Output Voltage V_o calculated V	Load Ohms
1	40	7.2	7.2	40
2	50	9.4	9	50
3	60	11.2	10.8	65
4	70	13	12.6	80
5	80	15.6	14.4	98

3. Constant VoltageV_{in}=15V ,Load Current I_l=0.13A

Table 3.6: Open Loop varying duty cycle 15V input

Sr.No	Duty Cycle%	Output Voltage V_o measured V	Output Voltage V_o calculated V	Load Ohms
1	40	5.6	6.0	30
2	50	7.4	7.5	47
3	60	9.4	9	70
4	70	10.6	10.5	78
5	80	11.6	12	84

The graphs for duty cycle versus measured and calculated voltage are plotted below in figure 3.33, figure 3.34 and figure 3.35 for the three voltage of 24V, 18V and 15V respectively.

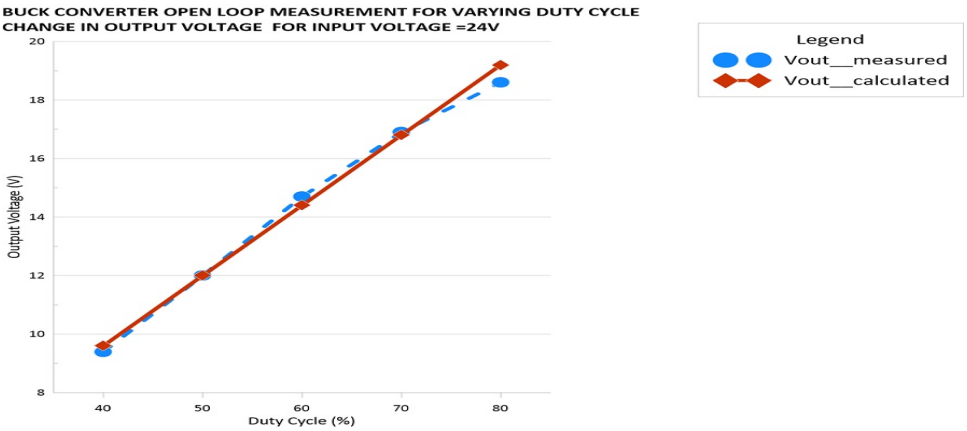

Figure 3.33: Buck Open loop measurement Vin=24V

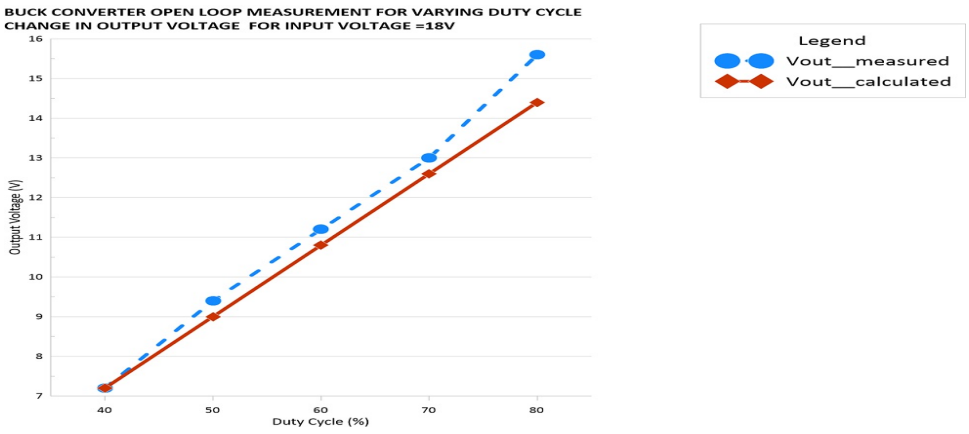

Figure 3.34: Buck Open loop measurement Vin=18V

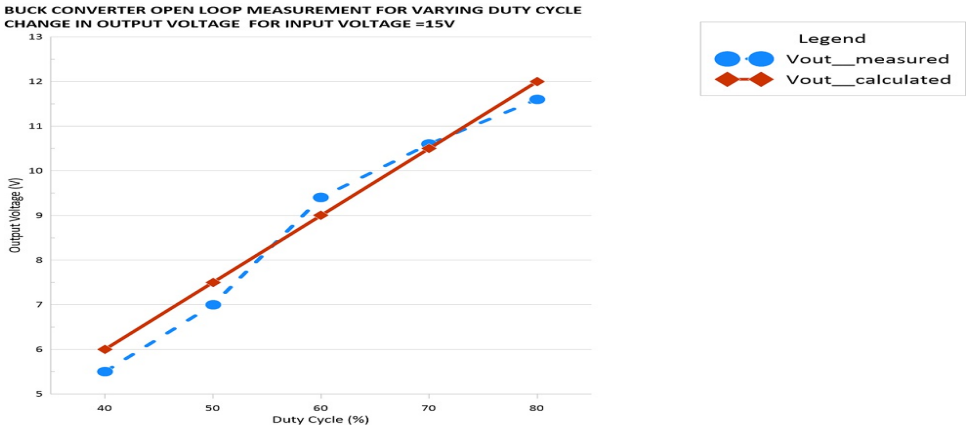

Figure 3.35: Buck Open loop measurement Vin=15V

Another set of readings are noted for a constant duty cycle and constant load current by varying the input voltage. The load is kept constant.Measurements are carried out with duty cycle ranging from 50% to 80%. Table 3.7 and table 3.8 show the measured and calculated values of the output voltage for varying duty cycle.

1) Duty Cycle=50%

Table 3.7: Open Loop varying input Voltage for 50%Duty Cycle

Sr.No	Input Voltage V_{in} V	Output Voltage V_o measured V	Output Voltage V_o calculated V	Load Current A
1	15	7.2	7.5	0.71
2	16	8.2	8.0	0.81
3	17	8.7	8.5	0.90
4	18	9.3	9.0	0.96
5	19	9.2	9.5	1.05
6	20	9.9	10	1.12
7	21	10.5	10.5	1.20
8	22	11.3	11.0	1.29
9	23	11.8	11.5	1.38
10	24	12.4	12.0	1.50
11	25	13.3	12.5	1.6
12	26	14.2	13.0	1.65
13	27	15.5	13.5	1.73
14	28	16.8	14	1.84

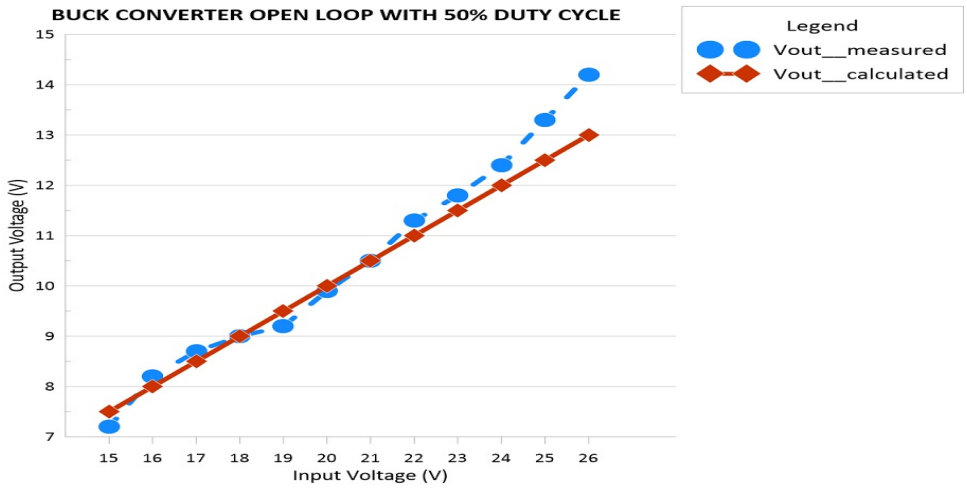

Figure 3.36: Buck Open loop measurement Duty Cycle=50%

2) Duty Cycle=60%

Table 3.8: Open Loop varying input Voltage for 60%Duty Cycle

Sr.No	Input Voltage V_{in} V	Output Voltage V_o measured V	Output Voltage V_o calculated V	Load Current A
1	15	8.2	9	0.72
2	16	9.1	9.6	0.82
3	17	9.8	10.2	0.97
4	18	10.5	10.8	0.98
5	19	11.2	11.4	1.09
6	20	12.1	12	1.20
7	21	12.8	12.6	1.27
8	22	13.6	13.2	1.38
9	23	14.4	13.8	1.48
10	24	15.9	14.4	1.59
11	25	16.7	15.0	1.70
12	26	17.7	15.6	1.82
13	27	18.5	16.2	1.91

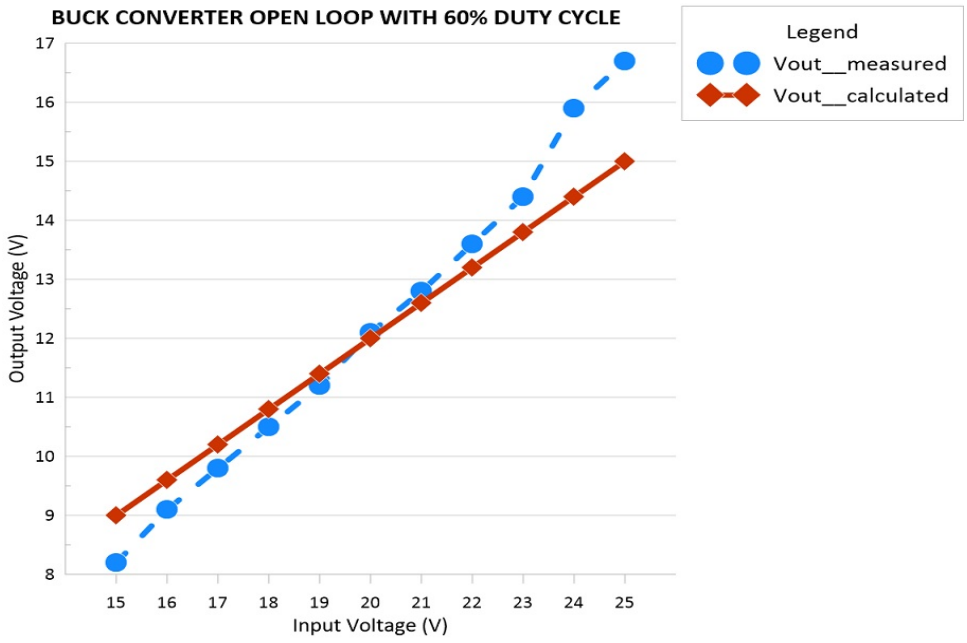

Figure 3.37: Buck Open loop measurement Duty Cycle=60%

The variations of input voltage versus output voltage for various duty cycles are plotted in figure3.36 and figure 3.37. It can be seen that for a open loop configuration, the output varies as the input changes or the duty cycle is varied. Hence, closed loop control is required for keeping the output regulated.

3.9.2 Closed Loop Configuration

The closed loop configuration is connected as shown in the schematic. The converter performance is analysed using closed loop control. The Finite state machine PI controller is downloaded on the FPGA. The constant of PI controller are set in the code itself. Also the reference value of the digital comparator was varied since the output resistors of the voltage divider were analog and had variation. Various values of q0 and q1 were tested and the following values were tuned.

1) q0=0000011 q1=1111111 Vref=2V named as PI constants=A

2) q0=0000111 q1=1111111 Vref= 2V named as PI constants=B

3) q0=0001111 q1=1111111 Vref= 2.2V named as PI constants=C

The Converter was tested for changes in the output voltage for 1) change in input voltage keeping load constant 2) change in load current keeping input constant The experimentation readings are tabulated below

A) Input Voltage was varied from 21V to 26V and the output voltage was measured for different PI constants.

Table 3.9: Closed Loop buck Converter output voltage for varying input voltage

Sr.No	Input Voltage(V)	Output Voltage(V)		
		PI constant A	PI constant B	PI constant C
1	21	11.4	11.3	11.3
2	22	11.7	11.6	11.5
3	23	11.9	11.7	11.8
4	24	12	12	12
5	25	12.3	12.5	12.1
6	26	12.5	12.7	12.3

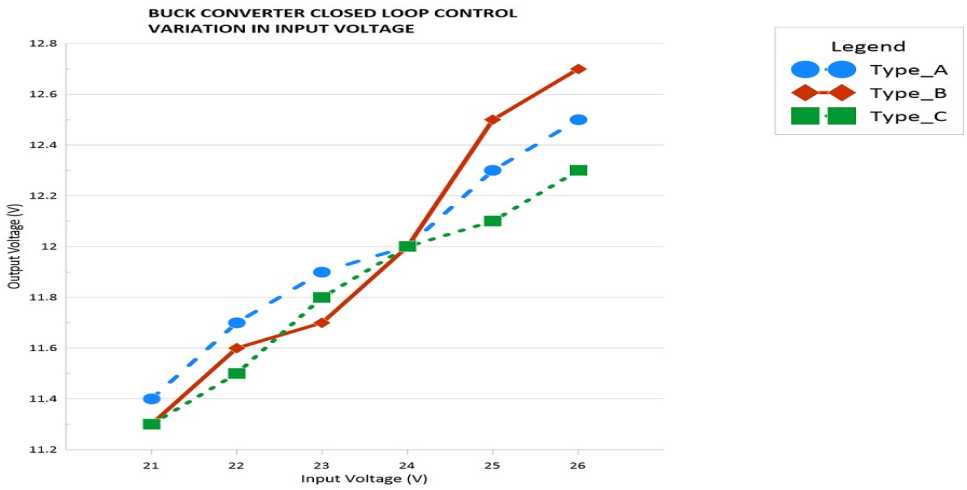

Figure 3.38: Buck Converter Closed loop variation in input voltage

The variation in the output voltage as input is varied is plotted in figure 3.38. It can be seen that the PI constant type C is having a linear range from 11.3V to 12.3V.

B)The output voltage was measured with changes in load current keeping input voltage constant. The experiment is repeated for all three PI constants for two input voltages 24V and 22V.

Table 3.10: Closed Loop varying Load Current for input voltage 24V

Sr.No	PI constant A		PI constant B		PI constant C	
	Load current A	Output voltage V	Load current A	Output voltage V	Load current A	Output voltage V
1	0.7	13	0.8	13.05	1.33	12
2	0.8	12.9	0.9	12.9	1.4	12.05
3	0.9	12.6	1	12.8	1.45	12.06
4	1.0	12.2	1.05	12.5	1.5	12.04
5	1.2	12.12	1.1	12.3	1.62	12
6	1.3	12.09	1.2	12.15	1.7	11.96
7	1.5	12	1.3	12.1	1.75	11.98
8	1.65	11.82	1.45	12.05	1.82	11.98

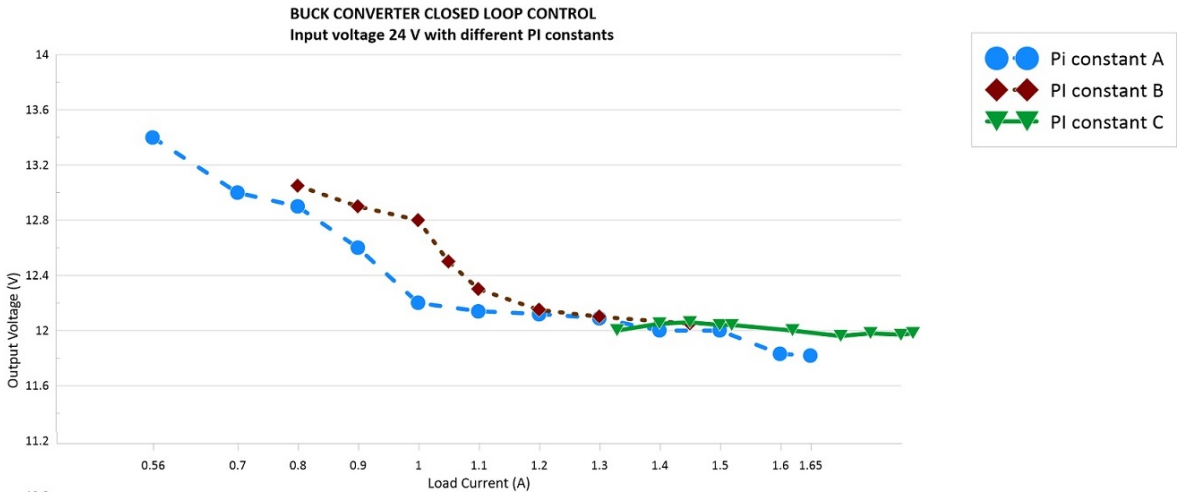

Figure 3.39: Buck Converter Closed loop output voltage variation for 24V input

Table 3.11: Closed Loop varying Load Current for input voltage 22V

Sr.No	PI constant A		PI constant B		PI constant C	
	Load current A	Output voltage V	Load current A	Output voltage V	Load current A	Output voltage V
1	0.56	12.5	0.7	12	1	12.13
2	0.6	12.35	0.8	11.95	1.1	12.06
3	0.8	11.89	0.9	11.9	1.2	12.04
4	0.9	11.65	1.0	11.75	1.3	12
5	1.03	11.45	1.1	11.2	1.4	12.07
6	1.12	11.35	1.2	11.1	1.5	11.8
7	1.27	11.25	1.3	11.05	1.6	11.9
8	1.4	11.2	1.45	11	1.7	11.9

Figure 3.39 and figure 3.40 show the closed loop control of a buck converter with PI control. It is observed that the constant type C gives a better control as compared to type A and type B. The stability factor, output resistance and the change in the output voltage is calculated for the converter with the three types of constants and is tabulated in table 3.12 It is observed that the PI controller having type C constants has the change in output voltage of 0.10 which is minimum thereby giving a better voltage regulation as compared to the other two constant types.

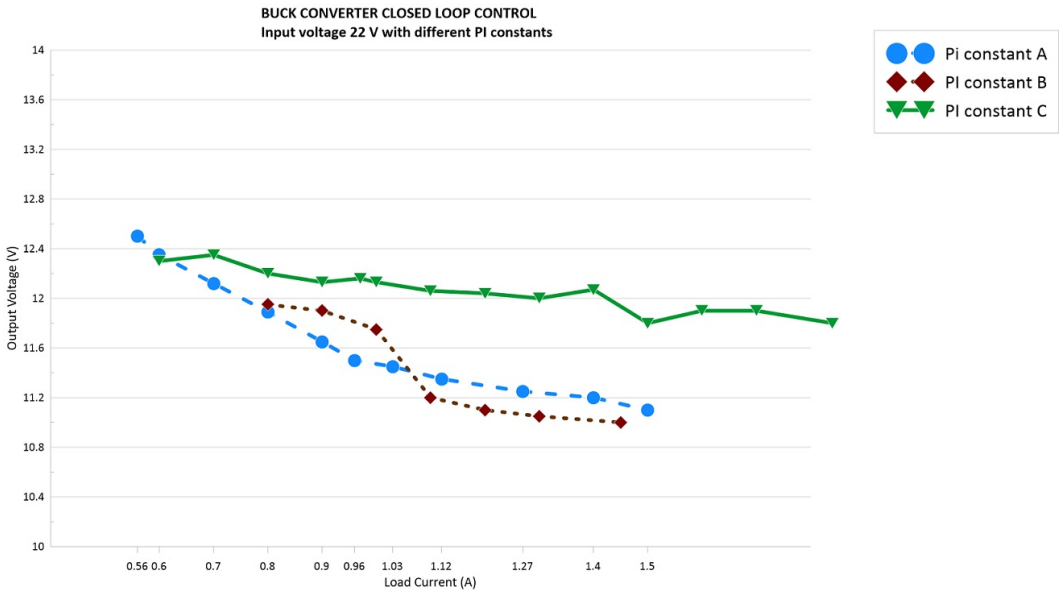

Figure 3.40: Buck Converter Closed loop output voltage variation for 22V input

Table 3.12: Performance Evaluation for Buck converter using PI controller

PI constant	Stability factor S_v	Output resistance $R_o(\Omega)$	Output Voltage Change $\Delta V_o/V_o$
A	0.22	1.55	0.20
B	0.28	1.33	0.21
C	0.2	0.33	0.10

The PID controller is also implemented on FPGA . The controller was tested with buck converter for closed loop control. The methodology for implementation remains same. The constants for this controller are tuned and the results obtained are as follows

1) q0=0001111 ,q1=1111100 and q2=0000111 Type D PID controller

2) q0=0001111 ,q1=1111100 and q2=0011111 Type E PID controller

The variations in the input voltage are plotted for the two types of constants as shown in figure3.41. The variation in the output voltage with changes in load current are plotted for buck converter with PID control for two different input voltages 22V and 24V as shown in the figure 3.42 and figure 3.43 Performance analysis is carried out for the PID controller for stability factor, output resistance and change in voltage as shown in table 3.13. It is observed that the stability factor of 0.073 is obtained for type D controller with 0.17Ω output resistance. The change in the output voltage is 0.06 which is better than the PI controller values.

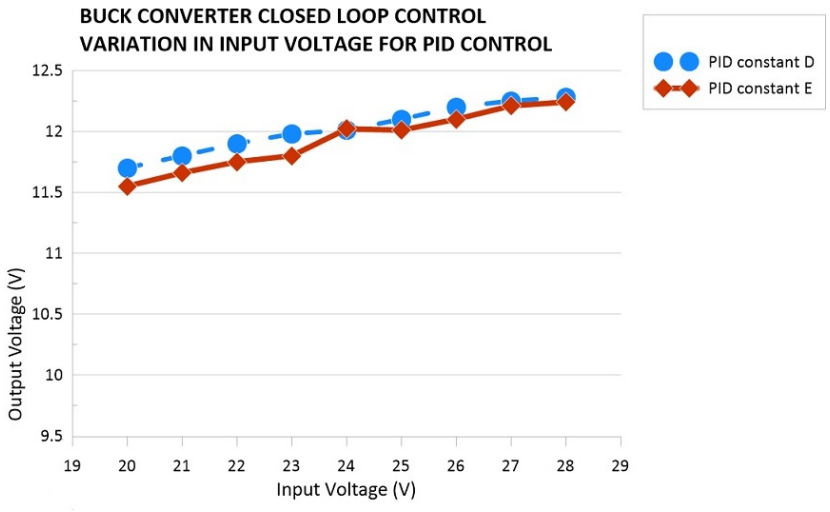

Figure 3.41: Buck Converter with PID control for variation in input voltage

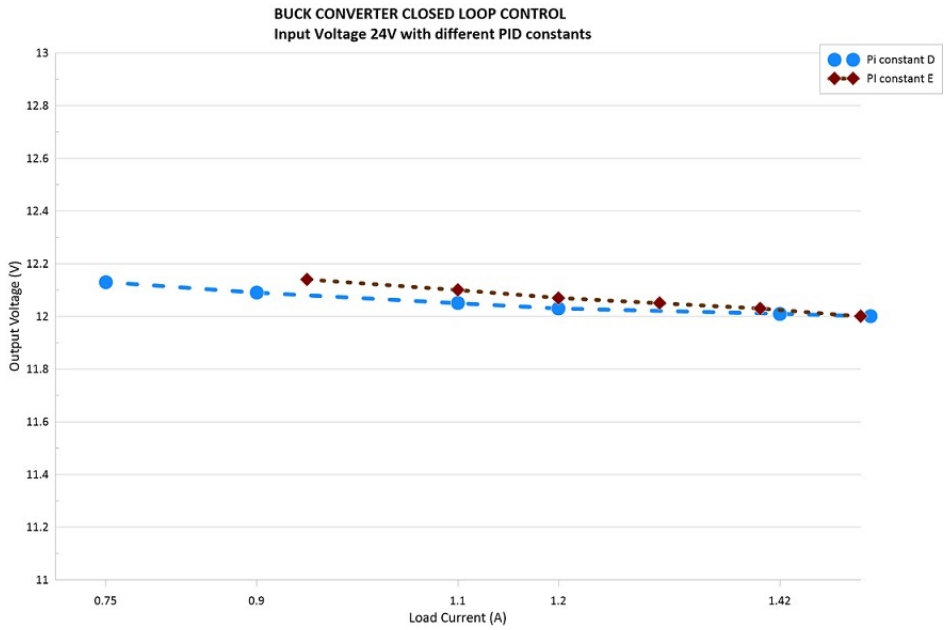

Figure 3.42: Buck Converter with PID control for changes in load with input voltage 24V

Table 3.13: Performance Evaluation for Buck converter using PID controller

PI constant	Stability factor S_v	Output resistance $R_o(\Omega)$	Output Voltage Change $\Delta V_o/V_o$
D	0.073	0.17	0.06
E	0.086	0.25	0.07

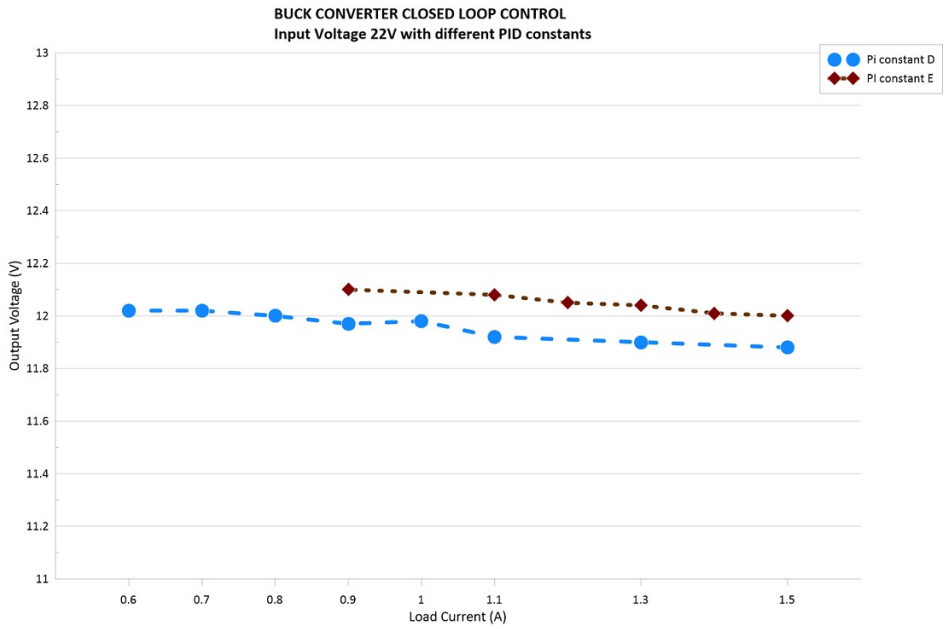

Figure 3.43: Buck Converter with PID control for changes in load with input voltage 22V

3.10 Conclusion

The analysis of the buck converter was performed with various aspects of the working, modeling, design, hardware implementation and outputs. Four types of compensators have been designed and the closed loop simulations are performed for buck converter. The PID controller emerges as a better control option, as demonstrated by the responses in the frequency and time domains. The stability boundary locus method is used to tune the analog controller parameters and obtain the equivalent discrete controller constants. Component selection was discussed and hardware was implemented. Buck converter using FPGA based control loop has been implemented with two types of controller viz. PI and PID. Performance evaluation has been performed for both open loop and closed loop configurations. It is observed that the closed loop configuration with type C PI constants leads to an optimal control of 0.1 variation of the output voltage. In a PID controller, the output voltage variation is 0.07 for type D. The PID controller provides better voltage regulation than the PI controller.

Chapter 4

Boost Converter with proposed Controller

4.1 Introduction

Boost Converter is used to convert the dc voltage from lower level to higher level. It is a step-up converter. Boost converters are used in automotives, power amplifiers, battery power systems, consumer electronics, dc motor drives and power factor correction circuits. They are used as point of load converters for driving high current loads in PCs and motherboards. The main components of a boost converter are switch, diode, inductor and a capacitor. The switch is controlled by a control signal generated by a controller. The controller maintains the constant output voltage of the boost converter. Working of a boost converter is elaborated. Converter transfer functions are derived using state space modeling approach. The converter is designed using the design equations. Hardware implementation with the components and the proposed VLSI based controller is tested for voltage regulation and performance is evaluated.

4.2 Working principle of Boost Converter

A boost converter is shown in figure 4.1 The input voltage source is connected to an inductor. The solid-state device which operates as a switch is connected across the source. The second switch used is a diode. The boost converter works on the principle of the tendency of an inductor to resist changes in current by either increasing or decreasing the energy stored in the inductor magnetic field. The inductor connected to input source leads to a constant input

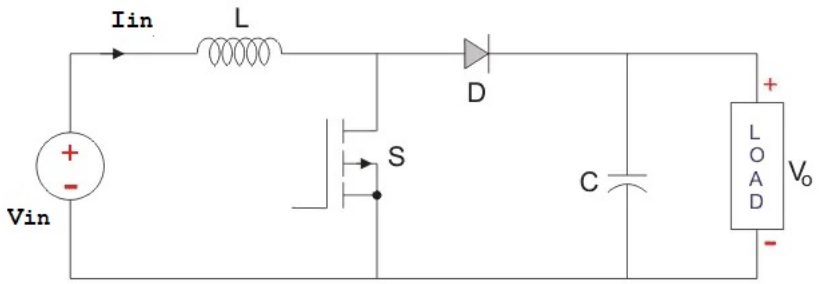

Figure 4.1: Boost converter

current, and thus the boost converter is also a constant current input source. The load can be seen as a constant voltage source. The controlled switch is turned on and off by using Pulse Width Modulation (PWM).

The working of the boost converter has two modes of operation. The first mode is shown in figure4.2(a).The switch is ON and therefore represents a short circuit ideally offering zero resistance to the flow of current so when the switch is ON all the current will flow through the switch and back to the dc input source. Let us say the switch is on for a time T_{on} and is

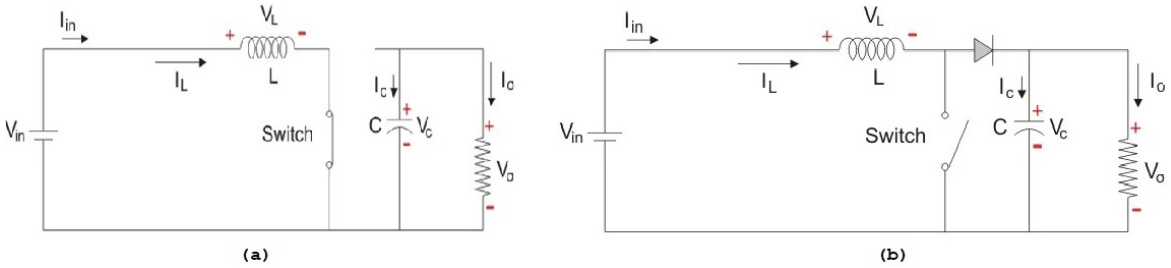

Figure 4.2: Boost converter working (a) Mode 1: switch closed (b) Mode2:switch open

off for a time T_{off}. The time period is given by

$$T = T_{on} + T_{off} \tag{4.1}$$

and the switching frequency f_s as

$$f_s = \frac{1}{T} \tag{4.2}$$

The duty cycle D is defined as

$$D = \frac{T_{on}}{T} \tag{4.3}$$

Analysis in steady state is done using KVL

$$V_{in} = V_L = L\frac{di_L}{dt} \tag{4.4}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT} = \frac{V_{in}}{L} \tag{4.5}$$

Since the switch is closed for a time T_{on}=DT

$$\Delta(i_L)_{closed} = \frac{V_{in}}{L} DT \tag{4.6}$$

The second mode is when the switch is open as shown in figure 4.2(b).The energy stored in the inductor is released and is ultimately dissipated in the load resistance, and this helps to maintain the flow of current in the same direction through the load and also step-up the output voltage as the inductor is now also acting as a source in conjunction with the input source.

Following is the analysis of the circuit in Mode 2 applying KVL.

$$V_{in} = V_L + V_o = L\frac{di_L}{dt} + V_o \tag{4.7}$$

$$L\frac{di_L}{dt} = V_{in} - V_o \tag{4.8}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{V_{in} - V_o}{L} \tag{4.9}$$

Since the switch is open for a time $T_{off} = T - T_{on} - T - DT = T(1-D)$, $\Delta t = T(1-D)$

$$\Delta(i_L)_{open} = \frac{V_{in} - V_o}{L}(1-D)T \tag{4.10}$$

The net change of the inductor current over anyone complete cycle is zero.

$$\Delta(i_L)_{closed} + \Delta(i_L)_{open} = 0 \tag{4.11}$$

Substituting the values,

$$\frac{V_{in}}{L} DT + \frac{V_{in} - V_o}{L}(1-D)T = 0 \tag{4.12}$$

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{4.13}$$

4.3 State Space Analysis

Modeling of boost converter is carried out in state space. The inductance current i_L and capacitance voltage V_o same as the output voltage are state variables. The state equations of the boost converter are obtained from the Mode 1 and Mode 2 .

From figure 4.2, applying KVL

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{4.14}$$

$$\frac{dV_o}{dt} = -\frac{V_o}{RC} \tag{4.15}$$

Putting these equations in the state equation given by

$$\dot{x(t)} = A_1 x(t) + B_1 V_{in}(t) \tag{4.16}$$

where A_1, B_1 imply mode 1 wherein switch is closed condition and i_L and V_o are the states x_1 and x_2 respectively. Substituting equations 4.14 and 4.15 in the state equation 4.16 ,we get

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_o} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} \tag{4.17}$$

During mode 2 as shown in figure 4.2, the following differential equations are obtained

$$\frac{di_L}{dt} = \frac{V_{in}}{L} - \frac{V_o}{L} \tag{4.18}$$

$$\frac{dV_o}{dt} = \frac{i_L}{C} - \frac{V_o}{RC} \tag{4.19}$$

Putting these equations in the state equation given by

$$\dot{x(t)} = A_2 x(t) + B_2 V_{in}(t) \tag{4.20}$$

where A_2, B_2 imply mode 2 wherein switch is open. Substituting equations 4.18 and 4.19 in the state equation 4.20 ,we get

$$\begin{bmatrix} \dot{i_L} \\ \dot{V_o} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} \tag{4.21}$$

The significance of state space averaging technique lies in replacing the above two sets of state equations by a single equivalent set described as follows,

$$\dot{x(t)} = Ax(t) + BV_{in}(t) \tag{4.22}$$

The A and B matrices are the weighted averages of actual matrices describing the switched system given by the following equations,

$$A = A_1 D + A_2(1 - D) \tag{4.23}$$

Substituting the values of A_1 and A_2 we get

$$\begin{aligned} A &= \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{RC} \end{bmatrix} D + \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} (1 - D) \\ &= \begin{bmatrix} 0 & -\dfrac{-(1-D)}{L} \\ \dfrac{1-D}{C} & -\dfrac{1}{RC} \end{bmatrix} \end{aligned} \tag{4.24}$$

$$B = B_1 D + B_2(1 - D) \tag{4.25}$$

$$B = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} D + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} (1 - D) = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} \tag{4.26}$$

The output equation is described by the following equation

$$y(t) = Cx(t) \tag{4.27}$$

where

$$C = C_1 D + C_2(1 - D) \tag{4.28}$$

hence substituting the values of matrix C, we get

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix} D + \begin{bmatrix} 0 & 1 \end{bmatrix} (1 - D) = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{4.29}$$

To solve steady state transfer ratios, the time derivatives are set to zero. The state equations are solved to get the steady state equations. Small perturbations in duty cycle D are assumed and the solution is obtained using Laplace transforms. The transfer functions are obtained as follows

$$\frac{V_o(s)}{D(s)} = \frac{V_{in}}{(1-D)^2} \frac{1 - s\dfrac{L}{R(1-D)^2}}{1 + s\dfrac{L}{R(1-D)^2} + \dfrac{s^2 LC}{(1-D)^2}} \tag{4.30}$$

Similarly, to obtain the transfer function of ratio of output voltage to input voltage following equation is obtained.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{1}{(1-D)} \frac{1}{1 + s\dfrac{L}{R(1-D)^2} + \dfrac{s^2 LC}{(1-D)^2}} \tag{4.31}$$

4.4 Boost converter Design

The parameters of boost converter are found using the following equations for inductor L and capacitor C [1].

$$L = \frac{V_{out} - V_{in}T(1-D)}{min(i_{load})} \tag{4.32}$$

where T is the time period and Δi_L is the peak to peak ripple current of the inductor.

$$C = \frac{V_o D T_s}{R \Delta V_o} \tag{4.33}$$

where ΔV_o is the peak to peak output voltage ripple. The parameters of buck converter are tabulated in table 1

Table 4.1: Boost Converter Parameters

Parameters	Design Value
Input Voltage V_{in}	5V
Output VoltageV_o	10V
Output Current I_o	2A
Max.Power Pmax	20W
Switching Frequency fs	50kHz
Inductor Current ripple Δi_L	0.5%
Output Voltage rippleΔV_o	10%
Inductor L	5mH
Capacitor C	20uF
Load Resistance R	5 Ohms

4.5 Boost converter simulation

The boost converter is simulated in Matlab Simulink with designed values. An open loop and closed loop simulation was performed and the output voltage and current were measured. Figure4.3 shows the simulink model of the open loop boost converter. The PWM signal is generated with the PWM generator block.

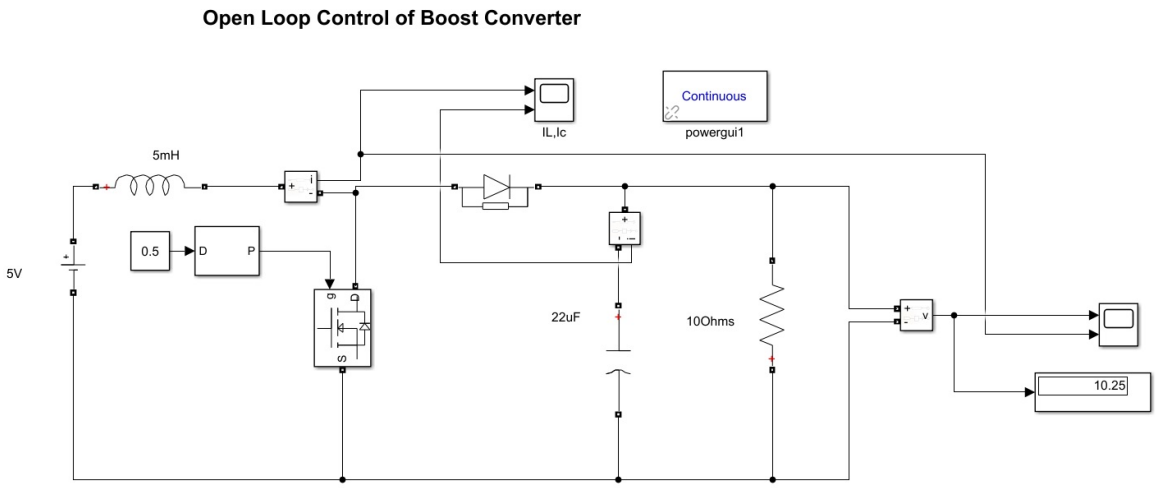

Figure 4.3: Open loop simulation of the boost converter

The design is simulated for 0.1s and the output is observed as shown in the figure 4.4. The output voltage is observed to be 10V and the current is 2A.

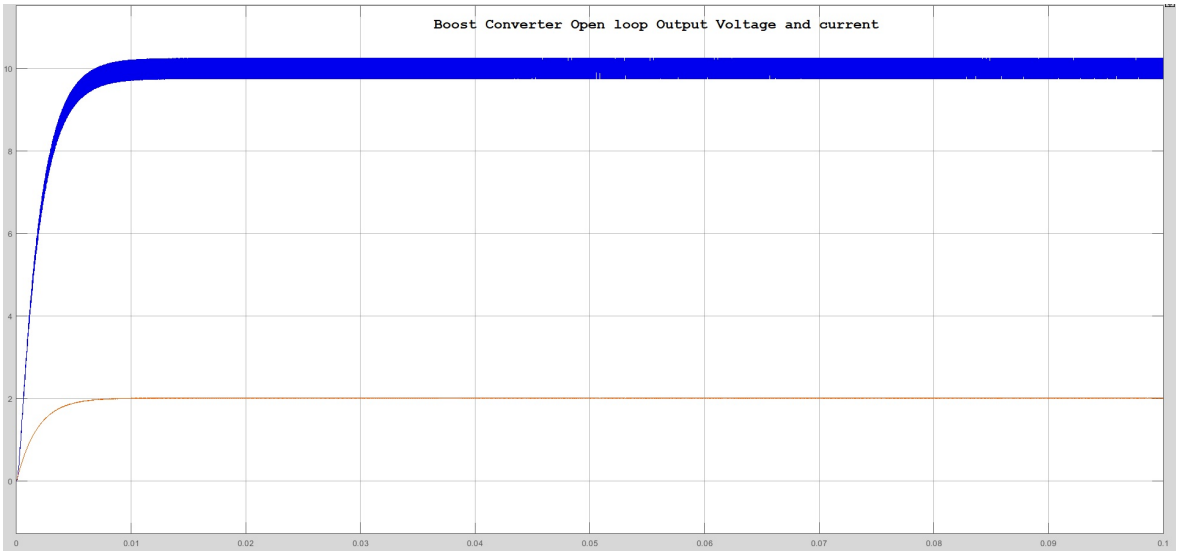

Figure 4.4: Output voltage and current for open loop boost converter Simulation

For optimal control, a closed loop boost converter is simulated. The Controller used is PI controller. The values of k_p and k_i are obtained using the Ziegler Nicholas technique. The values are 0.05 and 550. The simulation model is shown in figure 4.5. The closed loop path comprises of the reference and the error block, the PID discrete block and the PWM generator. The control signal generated drives the MOSFET.

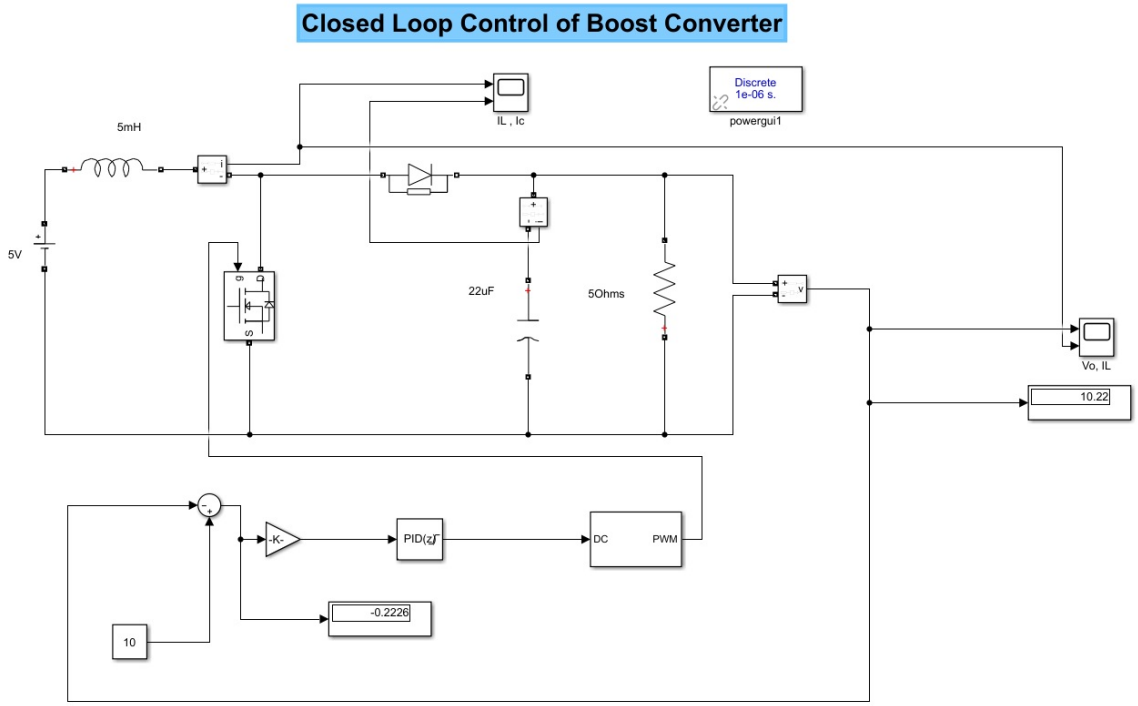

Figure 4.5: Closed loop simulation of the boost converter

The closed loop simulation output is shown in figure 4.6. The output is a steady output. The variations in the input voltage are shown wherein the controller adjusts the output to 10V.

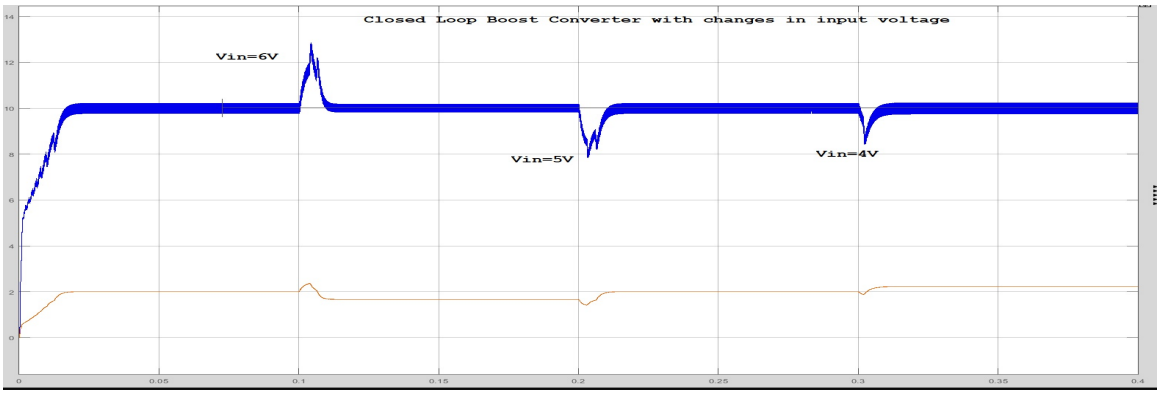

Figure 4.6: Output Voltage and current for changes in the input voltage of Boost Converter

4.6 Boost converter component selection

The boost converter is implemented using hardware components. The main components are inductor, diode, Power MOSFET, capacitor and load. The power supply is used to supply the

necessary input. The same components of buck converter with the design values of inductor and capacitor are used.

1. **Inductor**

   A ferrite core of 6mmX10mmX4mm was taken. Winding wire gauge SWG 26 with d=0.457mm was used and turns were 43. The core was wound and the inductance value of 5mH was checked on the LCR meter.

2. **Power MOSFET**

   The Power mosfet IRF520 along with heat sink was connected for heat dissipation.

3. **Power Diode**

   The diode selected was IN5822. It has 40V repetitive peak reverse voltage and 3A RMS forward current.

4. **Gate Driver**

   The driver IC FOD3184 was used as driver.

5. **Capacitor** A capacitor of 20μ F, 25V was chosen at the output stage.

6. **Resistors** A load of 10 ohm was taken at the output as load. Also the potential divider was connected to reduce the voltage to 2.4V

4.7 Hardware implementation

The hardware implementation of the boost converter is carried out and the FPGA based controller is interfaced with it. The set up is as shown in the figure 4.7. The PWM out from FPGA is connected to the driver IC FOD3184. The output of the FOD3184 is connected to gate of the MOSFET IRF520. The MOSFET is given the supply of 5V and the output of the drain is connected to the inductor and diode common terminal. The output of the converter is taken through a potential divider to the input of the ADC on FPGA board.

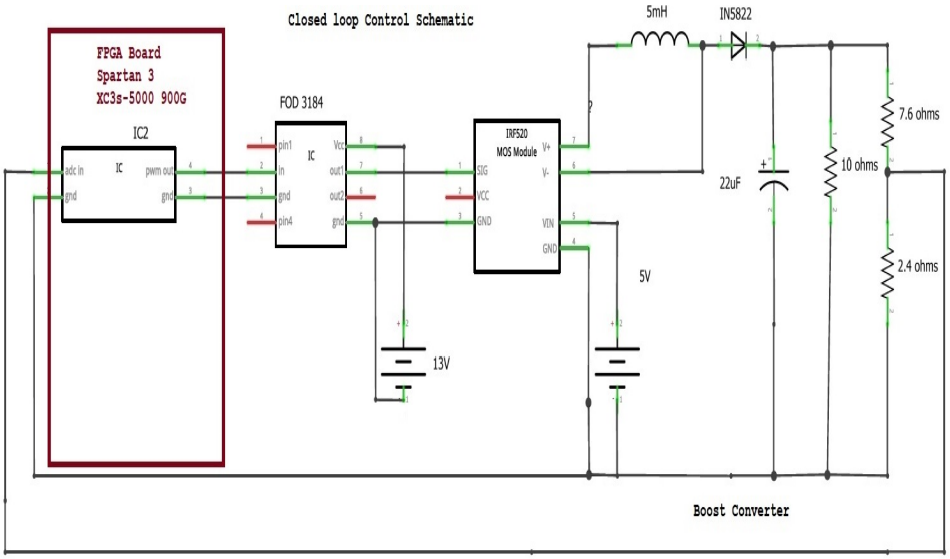

Figure 4.7: Hardware Implementation of the boost converter

4.8 Performance Evaluation

Boost converter is analyzed for open loop and closed loop performance. The input voltage, duty cycle and the load are the varying parameters. The evaluation is performed for stability and output resistance.

4.8.1 Open Loop Configuration

In the open loop configuration, a pulse width of varying duty cycle is generated using VHDL and downloaded on FPGA. The FPGA is programmed only for PWM output. The converter is given these pulses. The converter is subjected to constant input voltage keeping load current constant and observing the effect of varying duty cycle. Three sets of reading are taken and the variations are plotted.

1. Constant VoltageV_{in}=5V ,Load Current I_l= 0.12A

Table 4.2 shows the values of the output voltage for duty cycle varying from 60% to 20%. The measured value and the calculated value are recorded. The input voltage is 5V and the load current is kept constant at 0.12A

Table 4.2: Boost Converter Open Loop varying duty cycle 5V input

Sr.No	Duty Cycle%	Output Voltage V_o measured V	Output Voltage V_o calculated V
1	60	11.5	12.5
2	50	10.05	10
3	40	8.5	8.33
4	30	17.02	7.14
5	20	6.1	6.25

2. Constant VoltageV_{in}=4.5V ,Load Current I_l=0.11A

Table 4.3 shows the values of measured and calculated output voltage for input voltage 4.5V and load current of 0.11A with the duty cycle.

Table 4.3: Boost Converter Open Loop varying duty cycle 4.5V input

Sr.No	Duty Cycle%	Output Voltage V_o measured V	Output Voltage V_o calculated V
1	60	10.4	11.25
2	50	9.2	9.00
3	40	7.6	7.50
4	30	6.4	6.43
5	20	5.97	5.63

3. Constant VoltageV_{in}=5.5 ,Load Current I_l=0.13A

Table 4.4 shows the values of measured and calculated output voltage for input voltage 5.5V and load current of 0.13A with the duty cycle.

Table 4.4: Boost Converter Open Loop varying duty cycle 5.5V input

Sr.No	Duty Cycle%	Output Voltage V_o measured V	Output Voltage V_o calculated V
1	60	12.7	13.75
2	50	11	11.00
3	40	8.85	9.17
4	30	7.5	7.86
5	20	6.7	6.88

The measured and the calculated values of output voltage are plotted with respect to the duty cycle and are shown in figure 4.8, figure 4.9 and figure 4.10. The measured voltage and the calculated voltages are nearly similar from 20% to 50% but are slightly different for 60%.

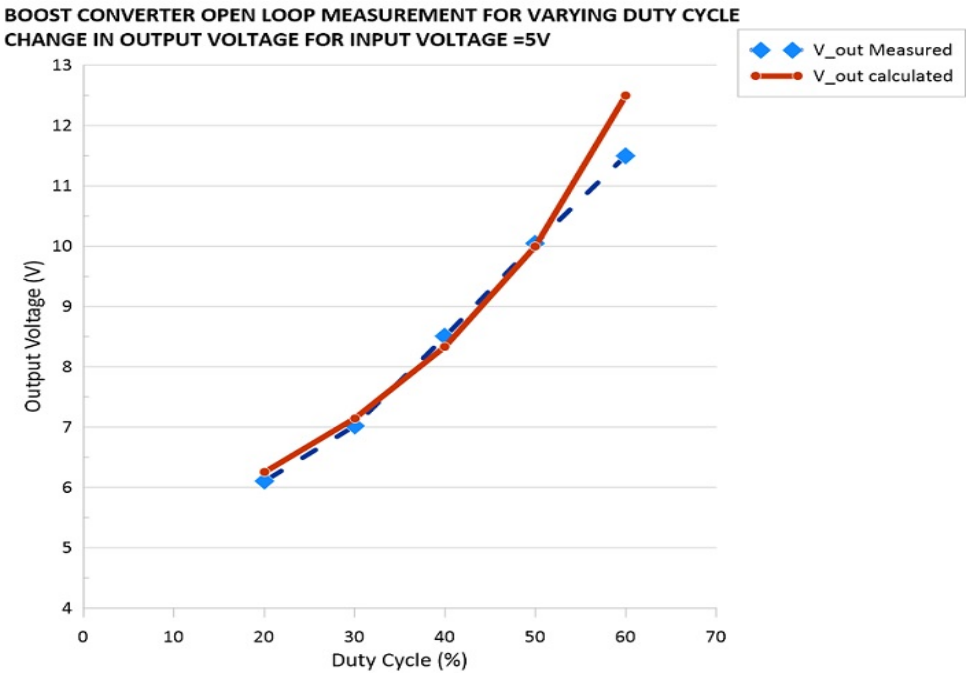

Figure 4.8: Boost Converter Open loop measurement Vin=5V

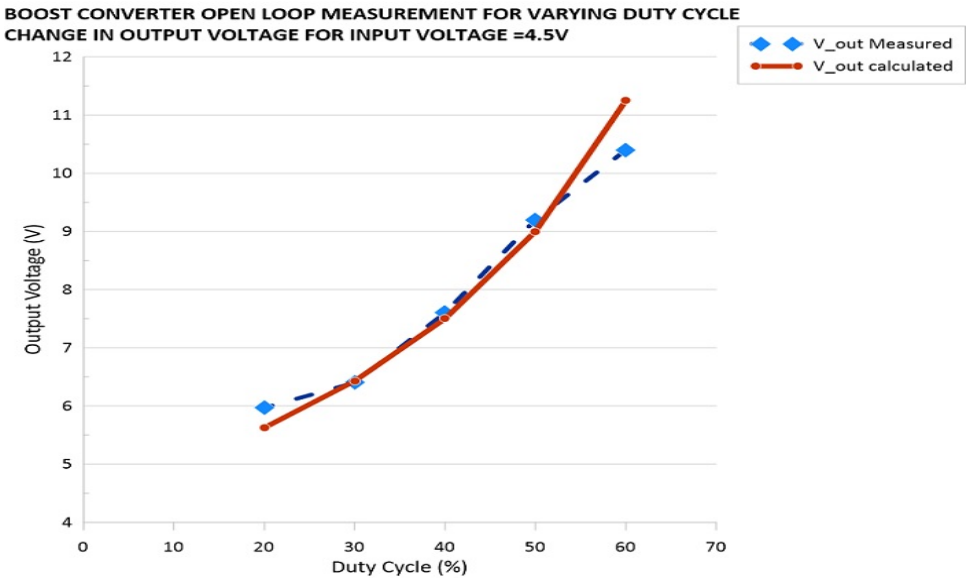

Figure 4.9: Boost Converter Open loop measurement Vin=4.5V

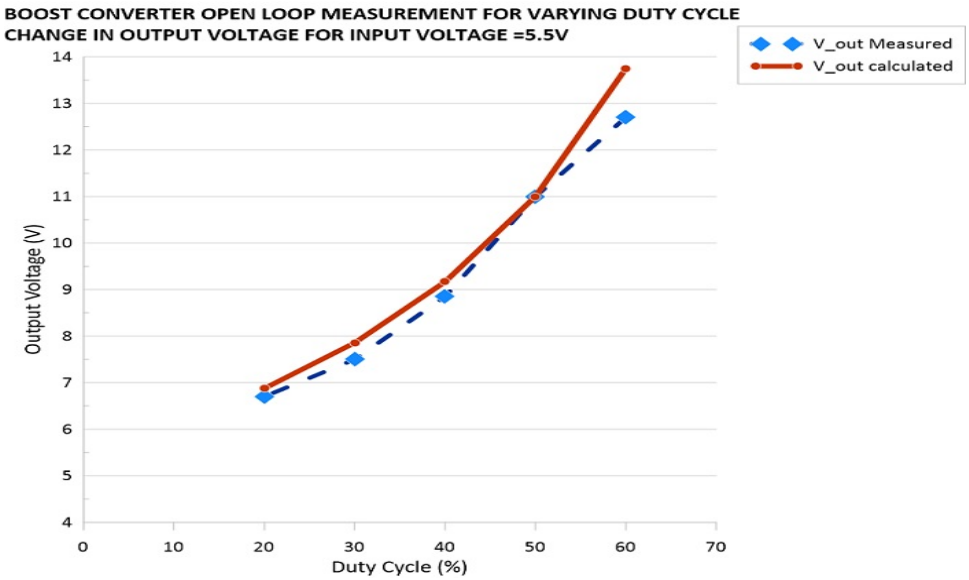

Figure 4.10: Boost Converter Open loop measurement Vin=5.5V

Another set of readings are noted for a constant duty cycle and constant load current by varying the input voltage. The load is kept constant.The output voltage is measured for change in input voltage . The output voltage is calculated for the duty cycle.The readings are tabulated in table 4.5- table 4.7. A comparison between the calculated and the measured output voltage is plotted for duty cycles from 60% to 40% shown in figure 4.11 - figure 4.13

1) Duty Cycle=60%

Table 4.5: Boost Converter Open Loop varying input Voltage for 60%Duty Cycle

Sr.No	Input VoltageV_{in} V	Output Voltage V_o measured V	Output Voltage V_o calculated V	Load Current A
1	5	11.5	12.5	0.12
2	4.9	11.2	12.25	0.12
3	4.8	10.8	12	0.12
4	4.7	10.65	11.75	0.12
5	4.6	10.58	11.5	0.12
6	4.5	10.4	11.25	0.11
7	4.4	10.1	11	0.11

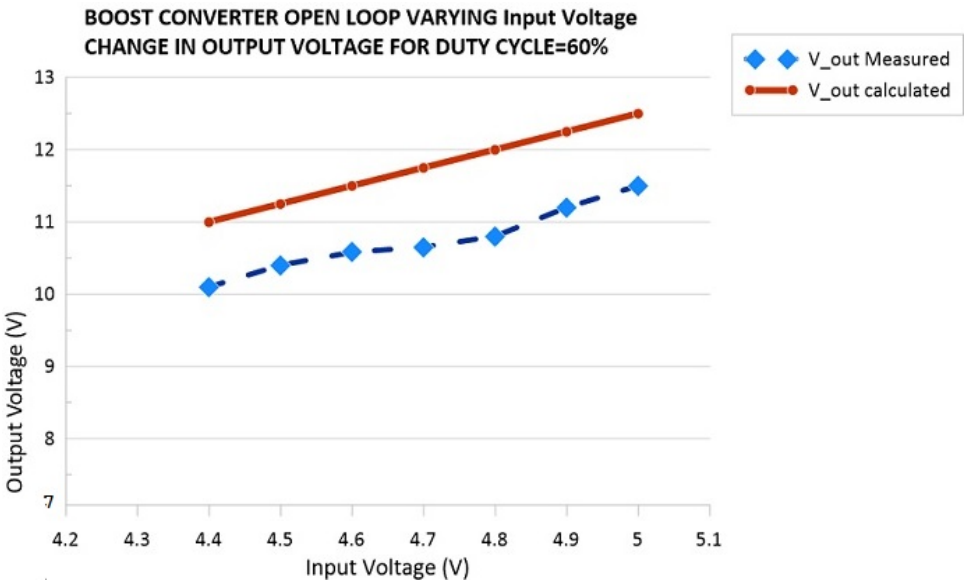

Figure 4.11: Boost Converter Open loop measurement Duty Cycle=60%

2) Duty Cycle=50%

Table 4.6: Boost Converter Open Loop varying input Voltage for 50%Duty Cycle

Sr.No	Input Voltage V_{in} V	Output Voltage V_o measured V	Output Voltage V_o calculated V	Load Current A
1	5	10.05	10	0.12
2	4.9	9.85	9.8	0.12
3	4.8	9.67	9.6	0.12
4	4.7	9.5	9.4	0.12
5	4.6	9.4	9.2	0.11
6	4.5	9.2	9	0.11
7	4.4	9	8.8	0.11

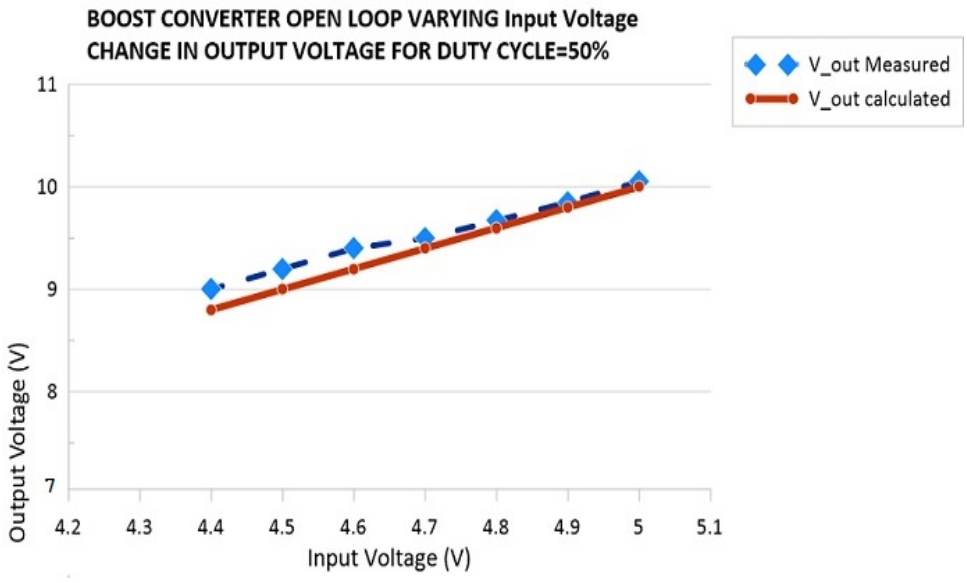

Figure 4.12: Boost Converter Open loop measurement Duty Cycle=50%

3) Duty Cycle=40%

Table 4.7: Boost Converter Open Loop varying input Voltage for 40%Duty Cycle

Sr.No	Input Voltage V_{in} V	Output Voltage V_o measured V	Output Voltage V_o calculated V	Load Current A
1	5	8.5	8.33	0.12
2	4.9	8.27	8.17	0.12
3	4.8	8.1	8.00	0.11
4	4.7	7.98	7.83	0.11
5	4.6	7.75	7.67	0.11
6	4.5	7.6	7.50	0.11
7	4.4	7.5	7.33	0.11

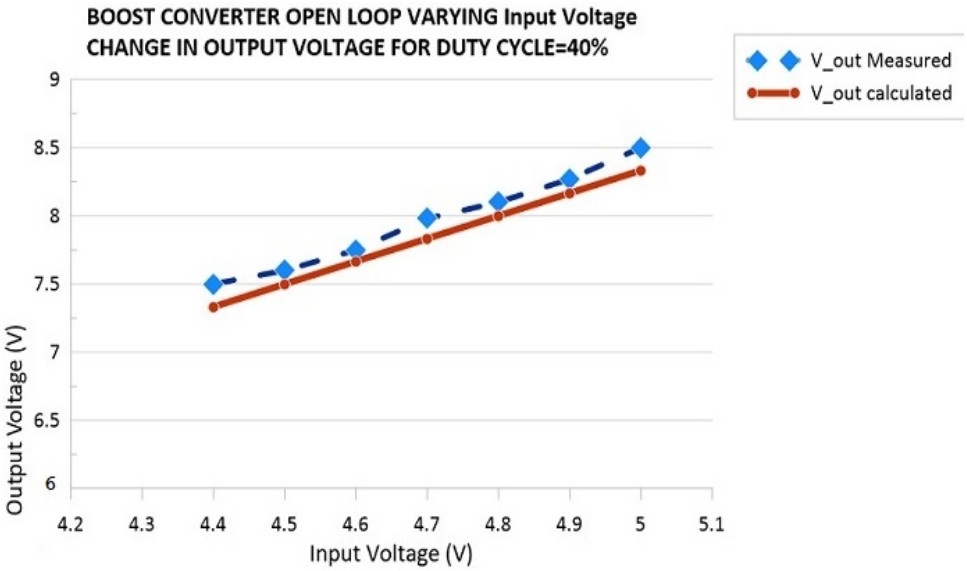

Figure 4.13: Boost Converter Open loop measurement Duty Cycle=40%

The open loop analysis shows the varying output with respect to the changes in duty cycle and changes in input voltage. A closed loop configuration ir required that will give a regulated output.

4.8.2 Closed Loop Configuration

An experimental setup similar to the buck converter is conducted. The PI constants were tuned to the analog values and the controller was downloaded onto the FPGA. The necessary changes were made to the PWM blocks and the comparator blocks in the program. Following PI constants were checked

1) q0=0011111 q1=01111111 Vref=3.0V named as PI constants=I

2) q0=0111111 q1=01111111 Vref=2.8V named as PI constants=II

The Converter is tested for changes in the output voltage for following conditions

A) Change in input voltage keeping load constant

Input voltage is varied from 4.7V to 5.5V and the output voltage is measured. The experimentation readings are tabulated in table 4.8 for the PI constant=I.

1) PI constants=I Load Current=0.17A

Table 4.8: Closed Loop Boost Converter varying input Voltage For PI constants=I

Sr.No	Input Voltage(V)	Output Voltage(V)
1	4.7	9.85
2	4.8	9.88
3	4.9	9.9
4	5	10
5	5.1	10.1
6	5.2	10.1
7	5.3	10.1
8	5.4	10.1
9	5.5	10.1

Table 4.9 shows a similar variation for PI constants=II

2) PI constants=II Load Current=1.45A

Table 4.9: Closed Loop Boost Converter varying input Voltage For PI constants=II

Sr.No	Input Voltage(V)	Output Voltage(V)
1	4.7	9.85
2	4.8	9.89
3	4.9	9.96
4	5	9.99
5	5.1	10
6	5.2	10
7	5.3	9.99
8	5.4	9.99

The variation in the output voltage as input is varied is plotted in figure 4.14 for both the constants. It can be seen that constant -II has a smaller variation in the output for change in the input.

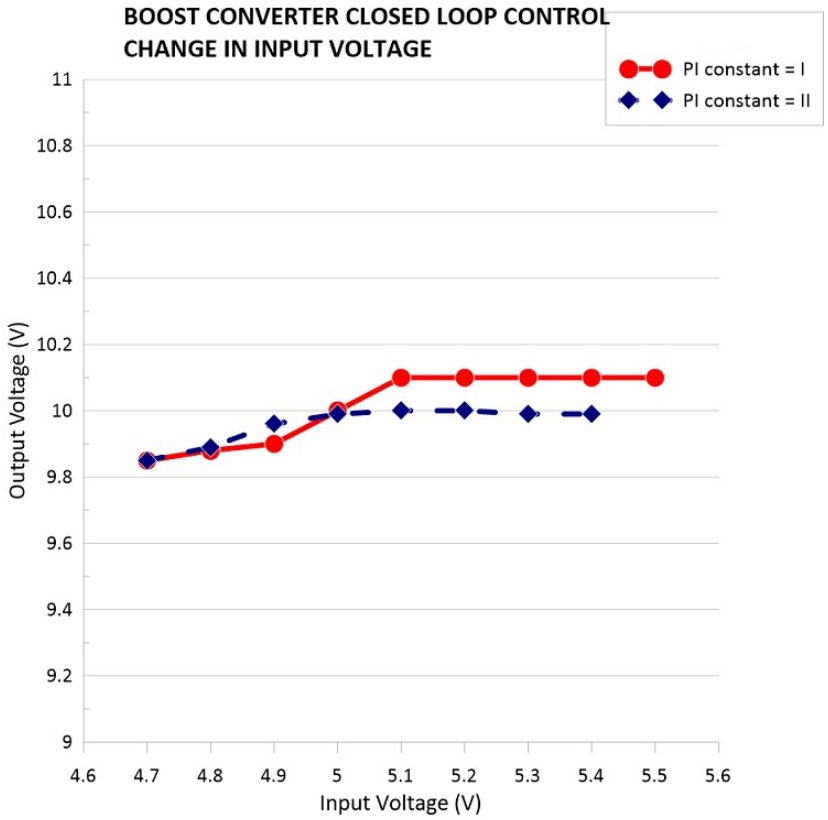

Figure 4.14: Boost Converter Closed loop variation in input voltage

B) Change in Output Voltage with change in load current for two values of input voltage 5V and 4.8V

1) Input Voltage =5V

Table 4.10: Closed Loop varying Load Current For Vin=5V

Sr.No	PI Constant =I		PI Constant =II	
	Load current (A)	Output Voltage(V)	Load Current(A)	Output Voltage(V)
1	0.15	10.1	0.14	9.82
2	0.16	10.08	0.15	9.75
3	0.17	10	0.16	9.73
4	0.18	9.8	0.17	9.64
5	0.19	9.6	0.18	9.58
6	0.2	9.58	0.19	9.4
7	0.21	9.4	0.2	9.35

2)Input Voltage =4.8V

Table 4.11: Closed Loop varying Load Current Vin=4.8V

Sr.No	PI Constant =I		PI Constant =II	
	Load current (A)	Output Voltage(V)	Load Current(A)	Output Voltage(V)
1	0.14	9.87	0.14	10.05
2	0.15	9.85	0.15	9.9
3	0.16	9.8	0.16	9.87
4	0.17	9.72	0.17	9.88
5	0.18	9.65	0.18	9.72
6	0.19	9.5	0.19	9.55
7	0.2	9.3	0.2	9.5

The variation in the output voltage for variation in load current is plotted.Figure 4.15 shows the the variation for input voltage 5V. Figure 4.16 shows the variation for input voltage 4.8V

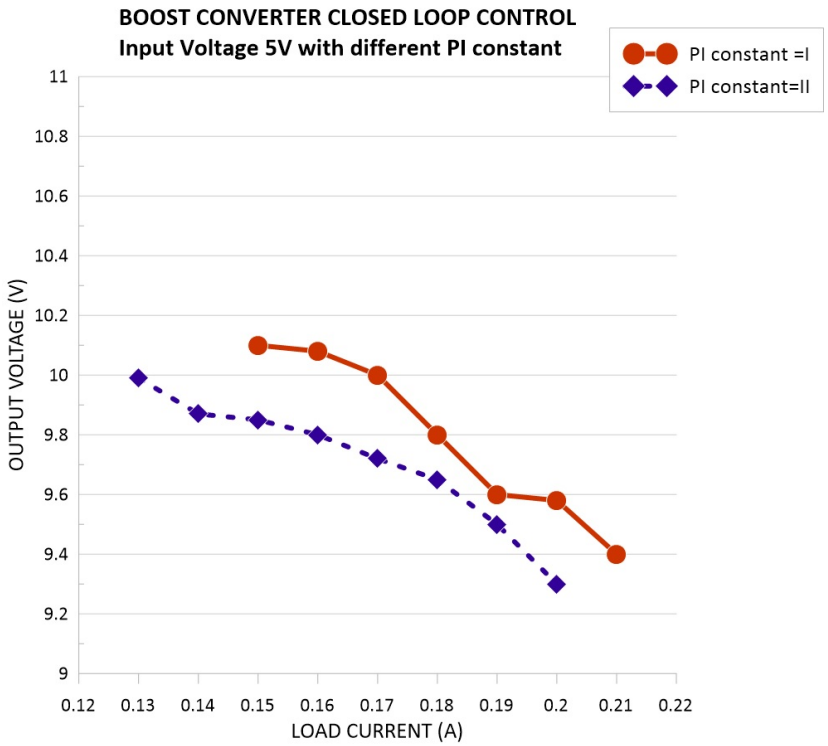

Figure 4.15: Boost Converter Variation in output voltage with change in load-Vin=5V

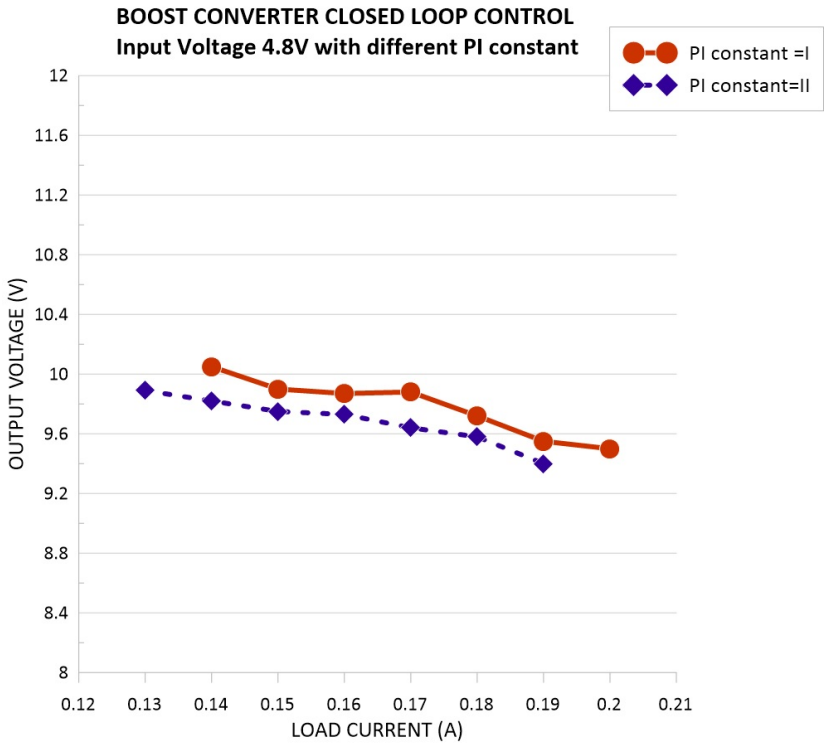

Figure 4.16: Boost Converter Variation in output voltage with change in load-Vin=4.8V

Performance evaluation was carried out for open loop and closed loop configuration of

a boost converter with PI controller. The stability factor, output resistance and the change in the output voltage is calculated for the converter with the two types of constants and is tabulated in table 4.12. It is observed that the closed loop configuration with constants PI=II give a better voltage regulation.

Table 4.12: Performance Evaluation for Boost Converter using PI controller

PI constant	Stability factor S_v	Output resistance $R_o(\Omega)$	Output Voltage Change $\Delta V_o/V_o$
I	0.031	11.6	0.10
II	0.042	7.8	0.05

4.9 Conclusion

Boost converter was analyzed with the proposed controller. The converter was also analyzed with state space modeling. Simulation of the open loop and closed loop converter was performed for PI controller in Matlab Simulink. Component selection and design of the components was carried out and the converter was tested for various conditions. The FPGA based PI controller with the feedback elements was designed and interfaced with the boost converter. Open loop and closed loop testing with hardware was performed to analyze the performance of the boost converter. Optimal control with PI constant II is achieved with a change of 0.05 in output voltage and is observed to provide excellent voltage regulation.

Chapter 5

FPGA based Controller Design

5.1 Introduction

FPGA technology is used in the field of telecommunications and image and signal processing. There is an increasing demand in the field of medical equipment, robotics , automotive and space and aircraft embedded control systems [18]. In this chapter, implementation of controllers on a FPGA platform is carried out. The controller and the additional blocks in the feedback loop i.e. digital comparator and pulse width modulator are also designed. The analog to digital conversion of the converter output is performed by an onboard ADC. Characteristics of a FPGA based controller are accuracy, reliability, programmability, fast time response and less space occupied. A PI controller is designed using three design styles. These are behavioral, structural and a finite state machine. A PID controller is also designed using a Finite state machine approach. VHDL coding language is used for design of the control loop. Simulations and synthesis i.e. the hardware generated are carried out using Xilinx ISE 14.7 Design suite.

5.2 FPGA Structure

FPGA is “Field Programmable Gate Array”. It contains ten thousand to more than a million logic gates with programmable interconnection. As shown in figure 5.1 FPGA consist of Configurable Logic blocks arranged in a matrix which are connected via a programmable switch matrix. The core is surrounded by programmable Input/ Output blocks. The memory cells control the logic blocks and the interconnects such that the desired functionality is implemented.

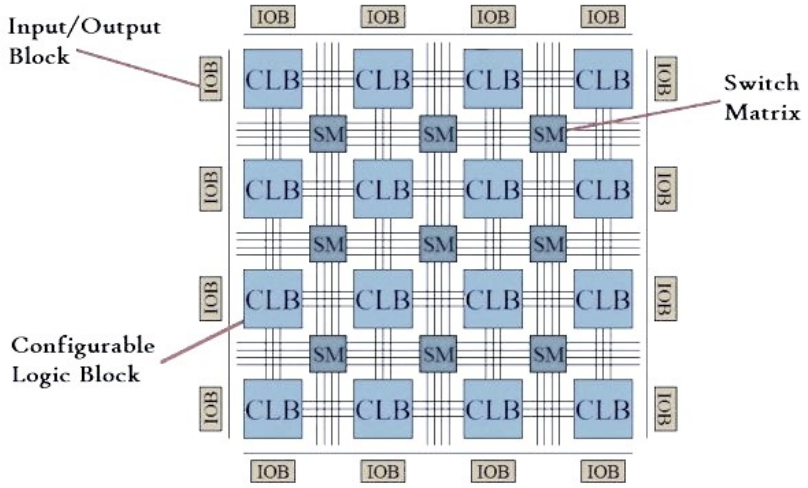

Figure 5.1: Structure of FPGA

FPGA have various resources available. These can be Random Access Memories (RAM), hardware accelerators, hard and soft processor cores etc. A logic block of a FPGA is shown in figure 5.2. It consists of a look up table (LUT), a carry look ahead block and a D-Flip Flop. The LUT has 4 bit input which has 16 combinations. A 16X1RAM or ROM memory or a combinational logic of 4 bit can be implemented in LUT. An arithmetic logic can be implemented with carry look ahead block. The logic can be sequential or purely combinational. A D type flip flop provides a registered output. Programmable interconnect connects many such logic blocks to implement a complex function .

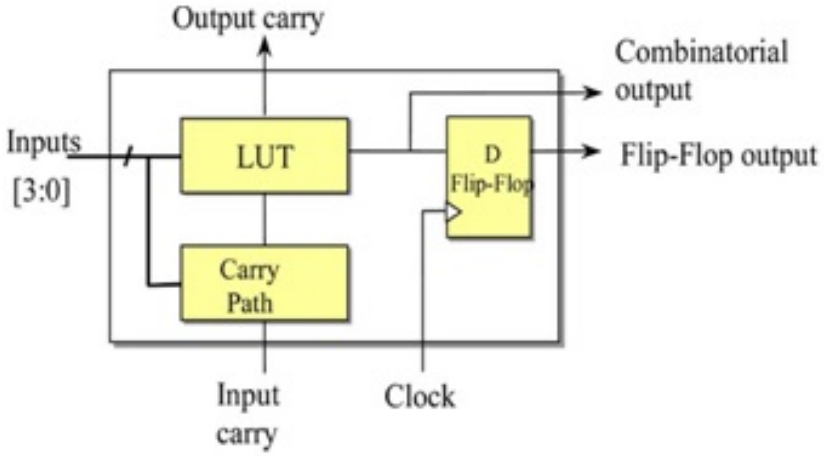

Figure 5.2: Logic block of a FPGA

The advantages of FPGA design is that it gives a concurrent logic. Sequential as well as combinational logic can be implemented with a parallel architecture, thereby increasing the speed of performance. High speed demanding algorithms can be efficiently implemented on

an FPGA.

FPGA's are programmed using Hardware description language (HDL).These are

1) VHSIC hardware description Language (VHDL)

2) Verilog.

HDL is technology independent. Once the algorithm is synthesized onto a FPGA, it can then be implemented on a chip. Application Specific Integrated circuits (ASIC's) are customized for a system. Speed and area optimization can be achieved with this approach. FPGA's are highly reliable and accurate.

However integration of ADC's is not available on FPGA. This drawback can be overcome by designing an ADC block on FPGA or interfacing an external ADC on the FPGA board.

5.3 VLSI design Flow

The VLSI design flow consists of a logical design and a physical design as shown in figure5.3.

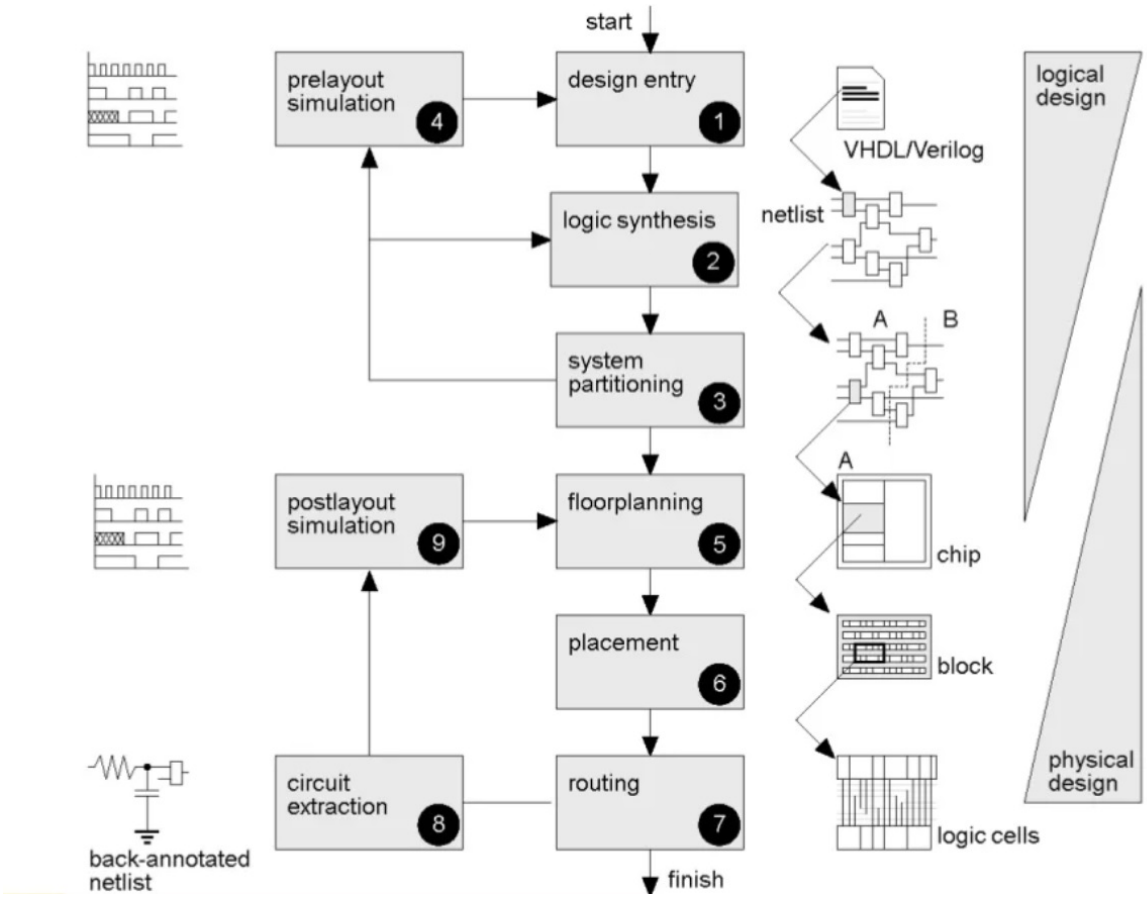

Figure 5.3: VLSI Design Flow

The first stage is the design entry in VHDL or Verilog coding. A hardware is developed using the synthesis tool and a prelayout simulation is carried out which is also called as the functional simulation. The design once verified is then layed out on the VLSI chip .The Spartan-3 XC3S5000-FG900 FPGA is selected and the layout –partitioning, floorplanning, placement and routing is carried out. The VHDL code is synthesized and simulated in the logical design and then it is physically implemented. A bit file is generated which can be downloaded on the FPGA . Xilinx14.7 ISE design suite is used to follow the procedure. The FPGA kit is interfaced by a JTAG support.

5.4 Methodology

The methodology used to design the feedback loop is shown in figure 5.4. A DC-DC converter is designed and implemented using hardware components. The output of the converter is taken as a feedback signal to a Analog to Digital converter(ADC) which is available on board and interfaced with the FPGA. The feedback loop blocks are Digital Comparator, PI controller, PMW generator are designed using VHDL Language and synthesized on the FPGA. The PWM output from the FPGA is used to trigger the switching MOSFET on the converter.

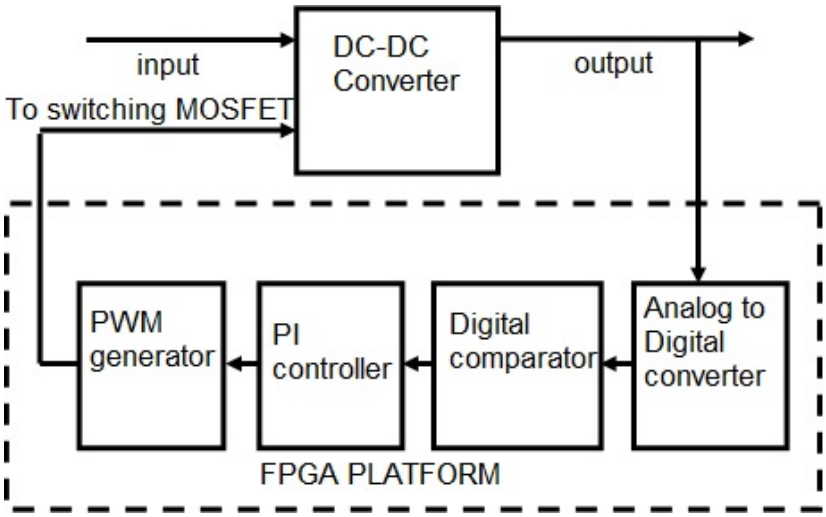

Figure 5.4: Methodology for the feedback loop on FPGA

All the blocks of the feedback loop are modeled using VHDL language. Spartan 3M FPGA design Board is used for implementing the design. Xilinx Project Navigator 14.7 is used to perform the various processes of synthesis and simulation. The simulation is ob-

served in ISim 14.7. The overall output is observed using the ChipScope Pro Logic Analyser. The various blocks of the feedback loop are described in the following section.

5.4.1 Analog to Digital Converter

The ADC used is AD9240 as shown in figure 5.5. It has a 14 bit digital output. It has a voltage range of 0-5V Sampling rate is 10 MSPS. The LSB of the ADC is calculated to

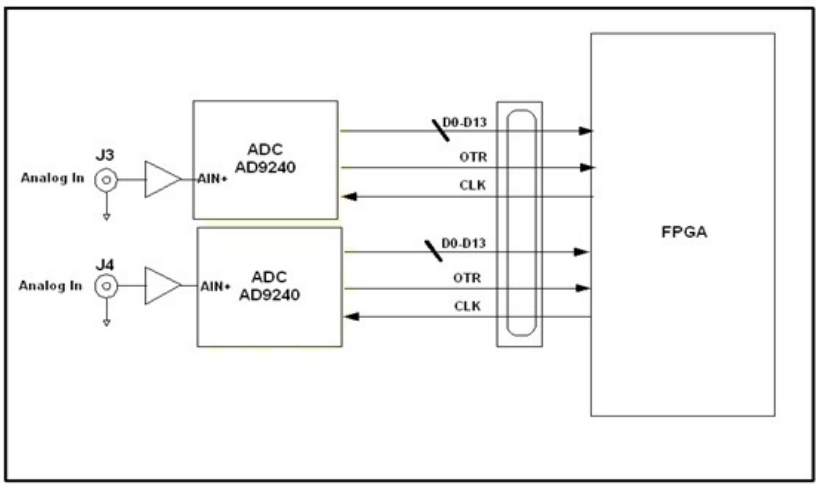

Figure 5.5: ADC interfacing with the FPGA

be 0.31mV. The maximum voltage it can measure is 4.999969V. The ADC is connected onboard. It has a analog input and it gives a digital output on the clock pulse. The output from the buck converter is reduced with the help of a potential divider to match the input voltage of the ADC. A VHDL code is written to get the 14 bit digital output onto the FPGA.

5.4.2 Comparator

The comparator block compares the digital output from the ADC with a reference. The comparator is designed to obtain the error signal. The reference is 2.4V i.e. (same as the divider output).It will generate an error which is the difference of two voltages. The error signal is unsigned positive number. The algorithm is as shown in figure 5.6. The 14 bit digital signal is compared to the reference. If the reference is greater than the digital signal, the error signal is the difference between the reference and the digital signal. A sign bit is set to 0. If the reference is less than the digital signal, the error signal is the difference between the digital signal and reference. The sign bit is set to 1. If reference and digital signal are

equal then error and sign bit is set to 0.

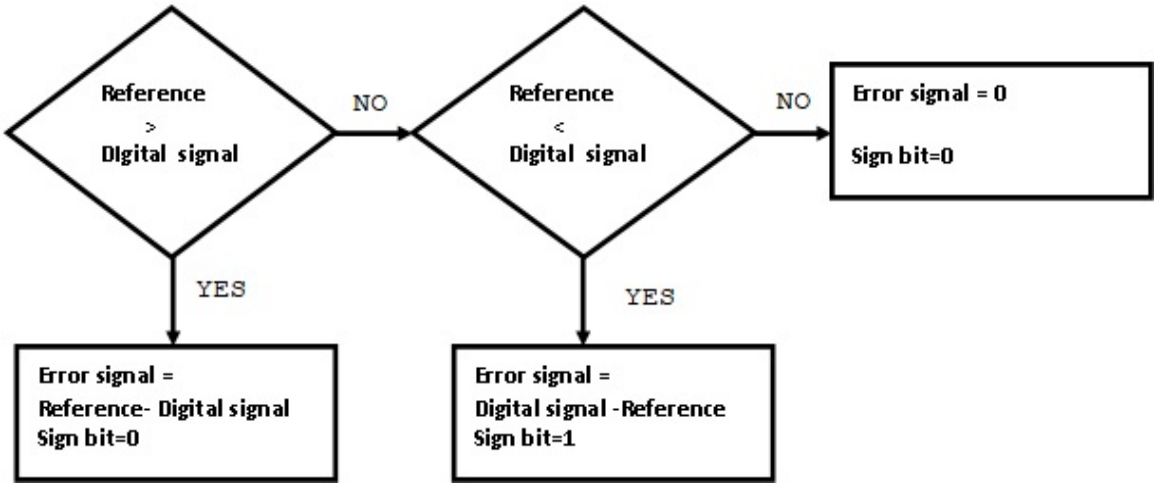

Figure 5.6: Comparator Algorithm

5.4.3 Pulse Width Modulator block

The PWM is achieved by comparing the output of the controller with a saw tooth wave. The PWM block is designed as shown in the figure 5.7. The frequency of the saw tooth wave is same as the converter frequency f_s. A counter in VHDL generates the necessary saw tooth waveform. The output of the controller is compared with the sawtooth waveform to generate a control signal which will switch the MOSFET.

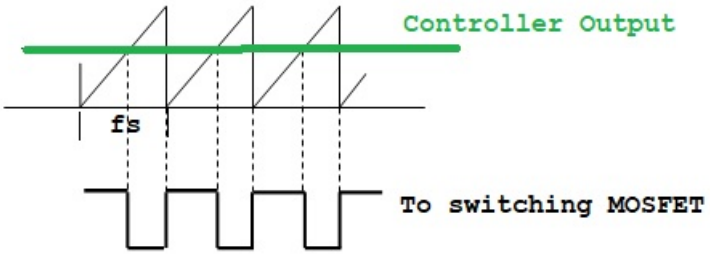

Figure 5.7: Pulse width modulator

5.5 Digital PI Controller

The traditional PI controller has the equation given by

$$u(t) = k_p[e(t) + \frac{1}{T_i}\int_0^t e(\tau)d\tau] \tag{5.1}$$

where k_p is the proportional gain, $T_i$is the integral time constant, e is the input and u is the output [38]. Modifying the equation for a sample time T in the discrete domain, following equation is obtained.

$$u(k) = k_p[e(k) + \frac{T}{T_i}\sum_{i=0}^{k-1} e(i)] \tag{5.2}$$

Similarly, u(k-1)can be obtained as follows

$$u(k-1) = k_p[e(k-1) + \frac{T}{T_i}\sum_{i=0}^{k-2} e(i)] \tag{5.3}$$

Subtracting equation5.3 from equation 5.2, a recursive PI control equation is obtained

$$u(k) - u(k-1) = k_p e(k) - k_p e(k-1) + k_p \frac{T}{T_i} e(k-1) \tag{5.4}$$

Thus, the discrete PI controller equation is obtained as follows

$$u(k) = u(k-1) + q_0 e(k) + q_1 e(k-1) \tag{5.5}$$

where q_0 =k_p and q_1=$-k_p(1 - \frac{T}{T_i})$
Thus the parameters of the analog controller can be converted in the discrete form using the above equations. There are three ways to model the PI converter in VHDL.

5.5.1 Behavioral modeling

In behavioral modeling , the behavior of the design is expressed using sequential statements. The modeling is at a very high level of abstraction. PI controller is modeled as a purely combinational logic. The hardware description code is written for the equation 5.5 using process statements and the output is observed.

5.5.2 Structural modeling

The PI controller is modeled using the parallel structure shown in figure 5.8. It shows multipliers, adders and registers. Parallel design implements decomposed equations obtained from equation 5.5

$$w_0 = q_0 * e(k) \tag{5.6}$$

$$w_1 = q_1 * e(k-1) \tag{5.7}$$

$$s_0 = w_0 + w_1 \tag{5.8}$$

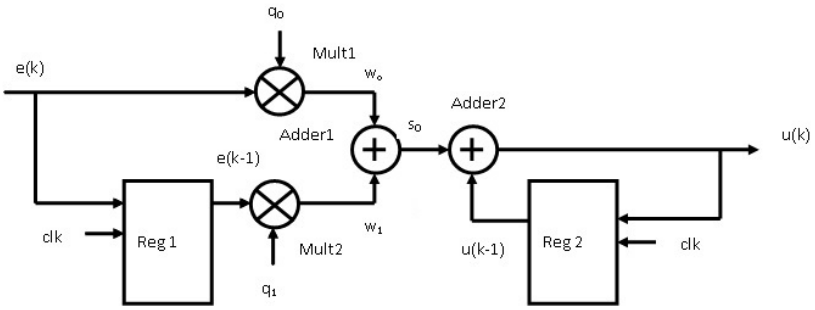

Figure 5.8: PI parallel structure

$$u_k = s_0 + u(k-1) \tag{5.9}$$

The error signal e(k) is multiplied by q_0 at multiplier block Mult1 to obtain w_0. e(k-1) is the delayed error signal of e(k) obtained at block Reg1. It is multiplied by q_1 at multiplier block Mult2 to obtain w_1 . The Adder1 block sums up the two multiplier outputs to obtain s_0 . u(k-1) is the delayed signal of u(k). The Adder2 block adds u(k-1) to s_0 , to obtain the output u(k).

5.5.3 Finite State Machine based modeling

Finite state machines (FSM) is a special modeling technique for sequential logic circuits. They are used in applications which operate in steps and have a defined task in each step. PI controllers have a output equation which has combinational as well as sequential logic. It also has a memory element which stores the previous value. There are two types of FSM -Mealy and Moore FSM. In a Mealy FSM ,the output is a function of the present state and the input whereas Moore has a output dependent on the present state only. The Finite state machine is a control strategy which has a state, an event and the necessary action. VHDL modeling has a defined sequence to generate a FSM. The PI controller is modeled using a finite state machine approach [42]. The discrete PI controller equation is given in equation5.5 The events occurring in the PI equation are of two time delays. One is e(k) and the other is e(k-1). This equation is put into 4 different states. To implement the PI structure, a finite state machine is designed as shown in figure 5.9 Referring to figure 5.9 state S0 represents the state when the system is at reset. State S1 is the state for q_0 multiplied with error e(k). State S2 is the state for q_1 multiplied with the delayed error e(k-1). State S3 is state where the equation is added and the final value is obtained at the output. The sequence of events is shown in table 5.1

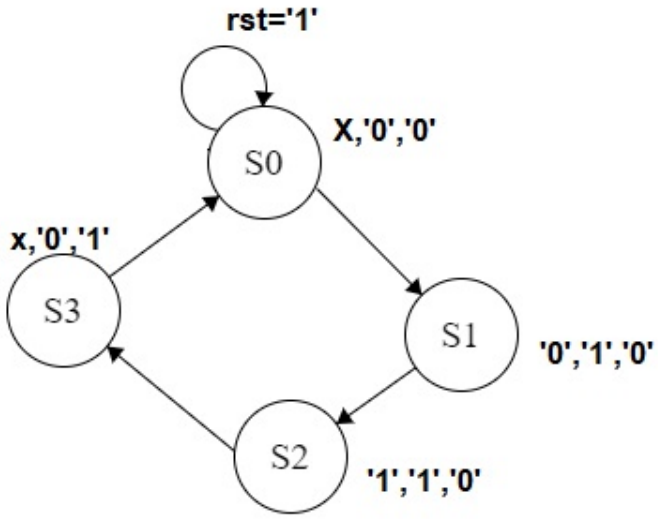

Figure 5.9: Finite State Machine for PI controller

Table 5.1: FSM sequence

State	Event	FSM Signals			
		Reset	sel	accreg	finreg
S0	RESET	1	X	0	0
S1	$q_0 * e(k)$	0	0	1	0
S2	$q_1 * e(k-1)$	0	1	1	0
S3	OUTPUT	0	X	0	1

The block diagram of the entire controller is shown in figure 5.10. The registers and controller are the sequential blocks whereas the adder, multiplier, multiplexer and the saturator are the data paths with combinational logic. The signals from the controller are used to feed in the multiplexer inputs for sel. The idreg is a continuous high signal to take in the error signal. The accreg is to add the three values and the finreg is to output the final value in the register. A saturator is required to limit the number of bits to 11. The output of saturator is given to the PWM block. The sign bit is checked here in the adder itself so that the required addition or subtraction can take place.

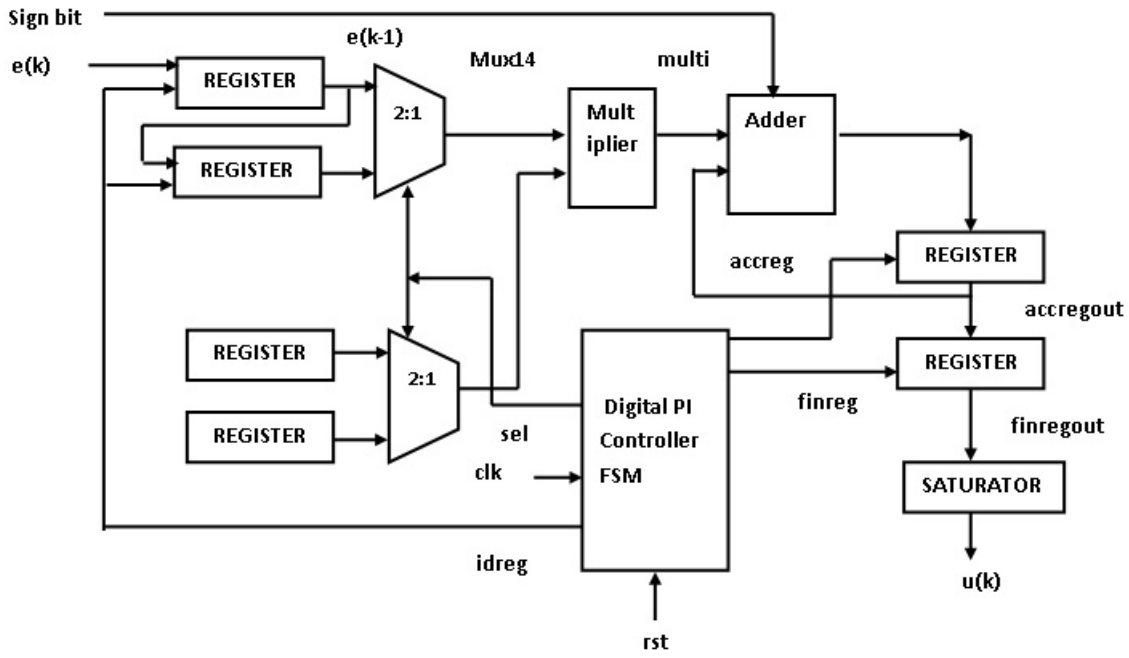

Figure 5.10: Block diagram of PI controller

5.6 Hardware of the control loop

Synthesis is the process of converting hardware description language into a netlist and mapping it on the programmable logic device. It will generate hardware blocks depending upon the library and the available resources. VHDL code is written for all the blocks and they are individually synthesized for hardware. The software used for design entry is Xilinx ISE Design Suite 14.7. It has the entire VLSI design flow of implementation. It also has a simulation tool to check the logical output by assigning input signals and checking the output.

The feedback loop on the FPGA platform is synthesized by coding individual blocks and then connecting them together to have a complete design. The modeling style used is structural modeling. The figure 5.11 shows the hardware generated. The blocks are instantiated in four instances. Input to the loop is the digital 14 bit value, clock and reset pin. Output of the block is the pwm signal generated and a divided clock of adc. The blocks are explained in detail with their hardware generated

1. Analog to Digital Converter

   The ADC synthesis is shown in figure 5.12. The ADC is onboard the FPGA and a VHDL code is written to capture the digital input generated to the pins of FPGA. The input voltage of the ADC is 5V. The converter output is taken from a voltage divider

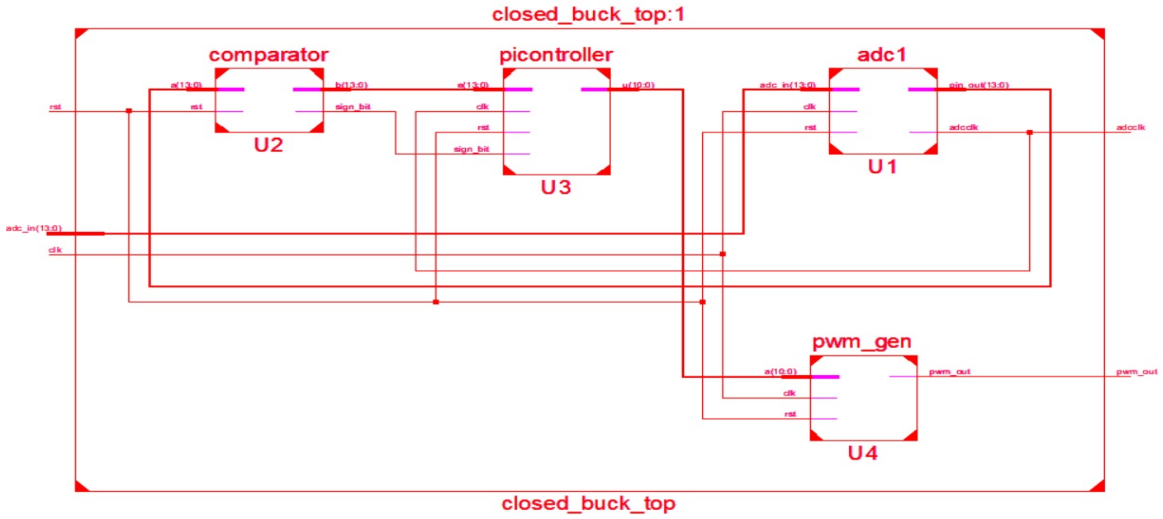

Figure 5.11: Synthesis of the feedback loop on FPGA

to reduce the voltage of output i.e. 2.4V. The ADC is driven by clock and reset. The sampling of the ADC is at 10MHz. Hence the on board clock is reduced to 10Mhz. The output of the ADC block is the 14 bit digital output and the divided clock signal.

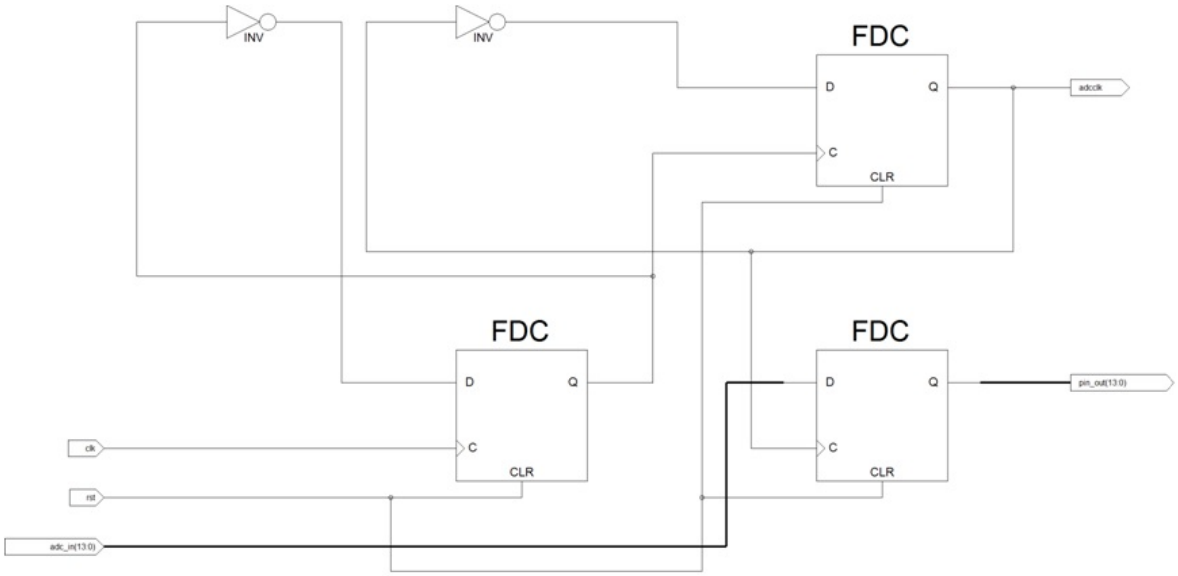

Figure 5.12: Synthesis of ADC block

2. Comparator

The digital comparator block is designed based on the behavioral modeling. Figure 5.13 shows the synthesis of the digital comparator. It has two inputs . The output of the analog to digital converter is one input. the second input is the reset signal. The

reference digital value is written within the code. A 2.4V reference signal is converted into a 14 bit digital value . The block shows comparator and addition and subtraction blocks. The output of the comparator is the error signal and the sign bit.

3. Pulse width Modulator(PWM)

   The PWM block has two parts. A counter is to be generated with the switching frequency. The saturated output of the controller is then compared with the counter value. If the saturated value is less than the counter, the output is low otherwise it is high. Accordingly the PWM output is generated. As shown in the figure 5.14, inputs to the block are the saturated value 11 bit, reset and clock. The output is a pulse width signal.

4. PI Controller. The PI controller is modeled using different design styles. The hardware generated of all 3 styles is also tabulated. The basic blocks are the registers, multiplier and the adder. The input is the 14 bit digital error and the output is a saturated compensated error signal. The clock and the reset are also required for the sequential logic. The proportional and the integral constants are written in the code itself.

   a) Behavioral modeling: Figure 5.15 shows the generated hardware. The behavioral coding is a high level coding and the synthesis is technology dependent. The multipliers, adders and registers are generated as shown in table 5.2. The hardware count gives a summary of the inferred logic and the number of the logic.

   Table 5.2: Device utilization for PI controller using behavioral modeling

Cell usage	PI behavioral
14x8-bit multiplier	2
14-bit adder	1
22-bit addsub	1
14-bit register	2
22-bit register	4

   b) Structural Modeling : In this type of modeling, the various blocks of a PI are generated individually and then connected in the top level HDL code. The basic blocks are latch, multipler, adder saturator. The hardware generated is shown in figure 5.16.

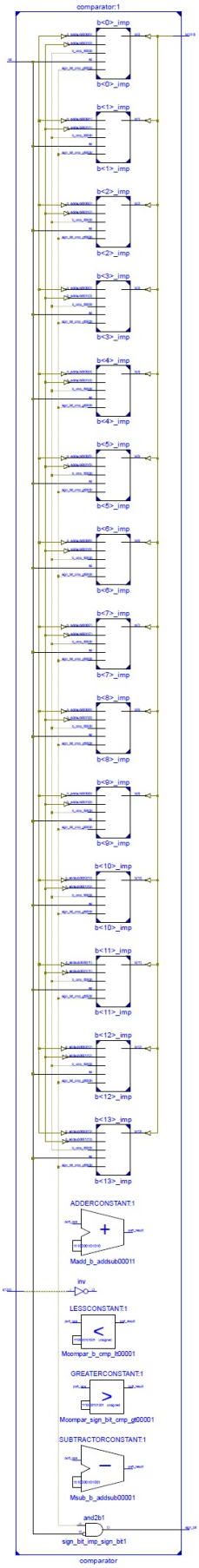

Figure 5.13: Synthesis of Comparator block

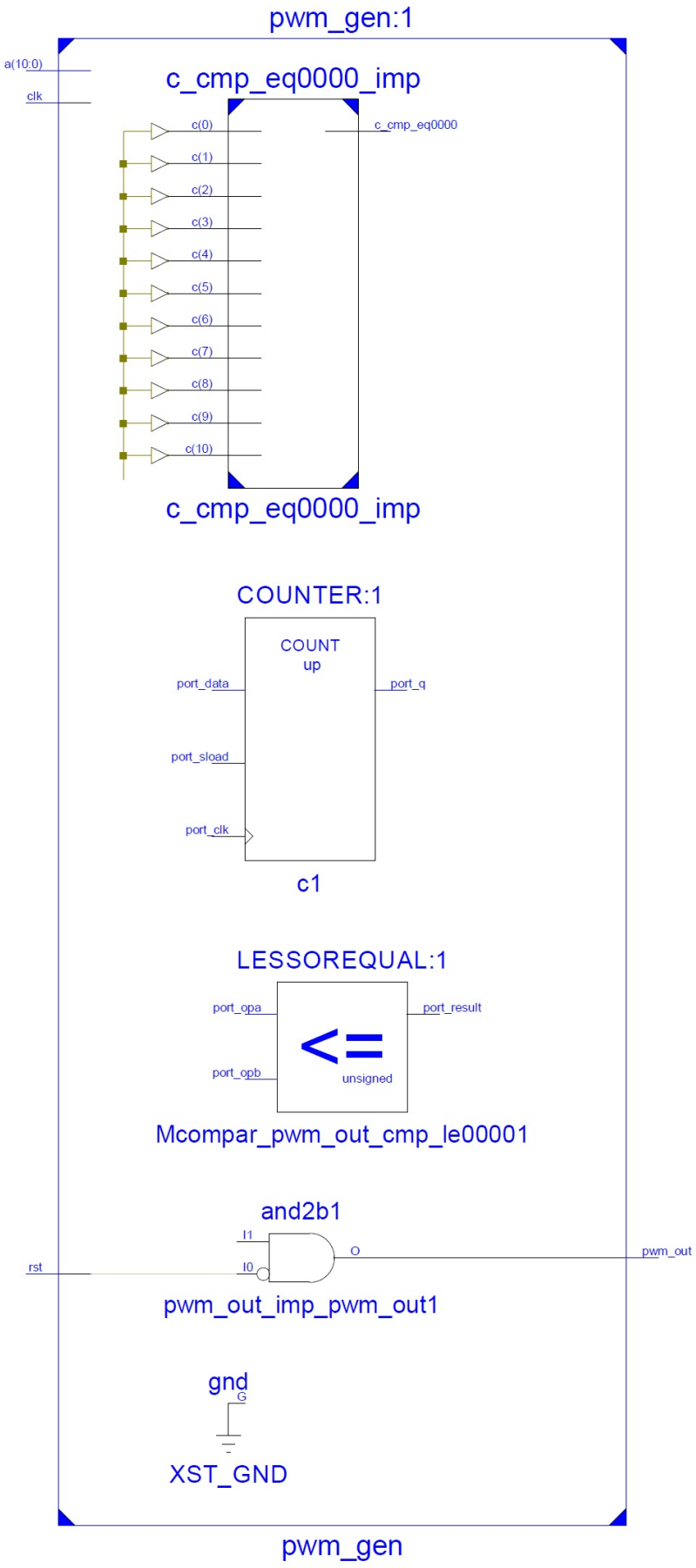

Figure 5.14: Synthesis of PWM block

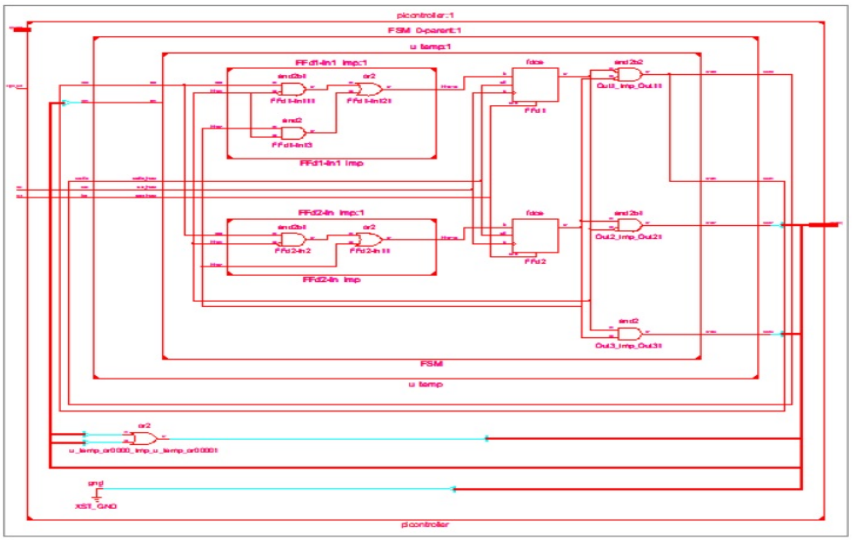

Figure 5.15: PI Behavioral Synthesis

Table 5.3: Device utilization for PI controller using structural modeling

Cell usage	PI structural
14x8-bit multiplier	2
23bit adder	3
14-bit register	1
22-bit register	1

The hardware count is shown in table 5.3. It can be seen that there is a reduction in the logic achieved using a structural modeling approach

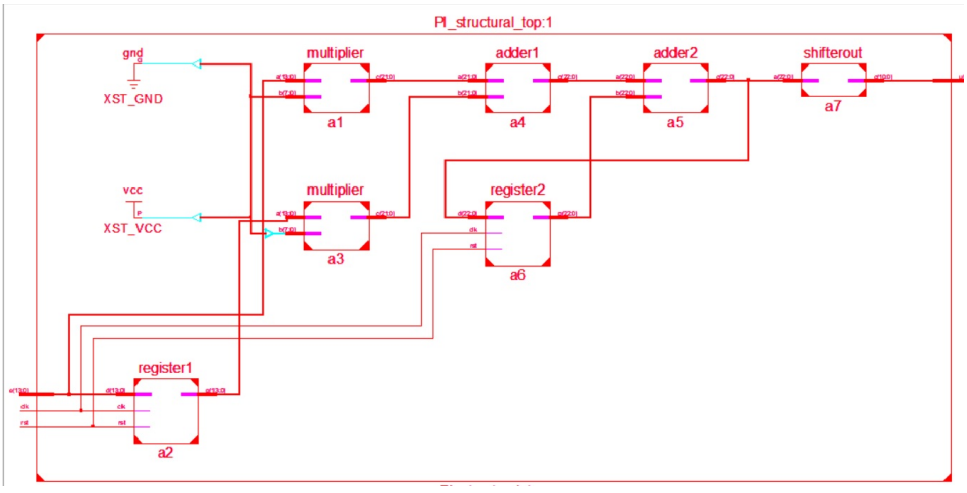

Figure 5.16: PI Structural Synthesis

3) Finite State Machine : Finite state machine (FSM) is an efficient method of designing a logic with data path and sequential path separated . The states are triggered in a sequential form and the output is obtained. The hardware generated is as shown in figure 5.17. It shows the datapaths with the registers, multipliers, saturators, adders. The sequence is generated with the FSM controller block. The hardware generated and the count is shown in table 5.4.It can be seen that a FSM with 4 states is inferred along with adder and subtarctor, multiplier and 14 bit and 22 bit register.

Table 5.4: Device utilization for PI controller using FSM

Cell usage	PI FSM Proposed design
FSM states	4
14x7-bit multiplier	1
22 bit adder	1
22 bit subtractor	1
14-bit register	2
22-bit register	2
No. of slice flipflops	66
No.of slice LUT	81

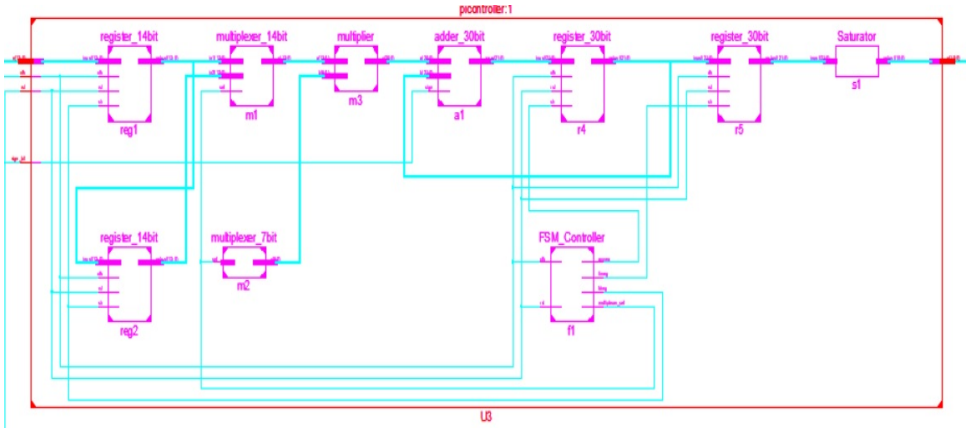

Figure 5.17: PI FSM Synthesis

5.7 Simulation

Simulation is the behavior of the circuit in terms of input signals and the output signals. The behavior is described in terms of occurrences of events and waveforms on signals. In this mode, design description is compiled and simulated. The results obtained are evaluated.

Simulations are performed individually on each of the blocks using the ISim simulator of ISE Design Suite 14.7. Each block is simulated for the various inputs and the output is checked. The overall controller is simulated for values of ADC 14 bit digital signal and the PWM output is shown in figure 5.18 The simulation is performed with low reset signal and two values of ADC output. The PWM signal generated is highlighted.

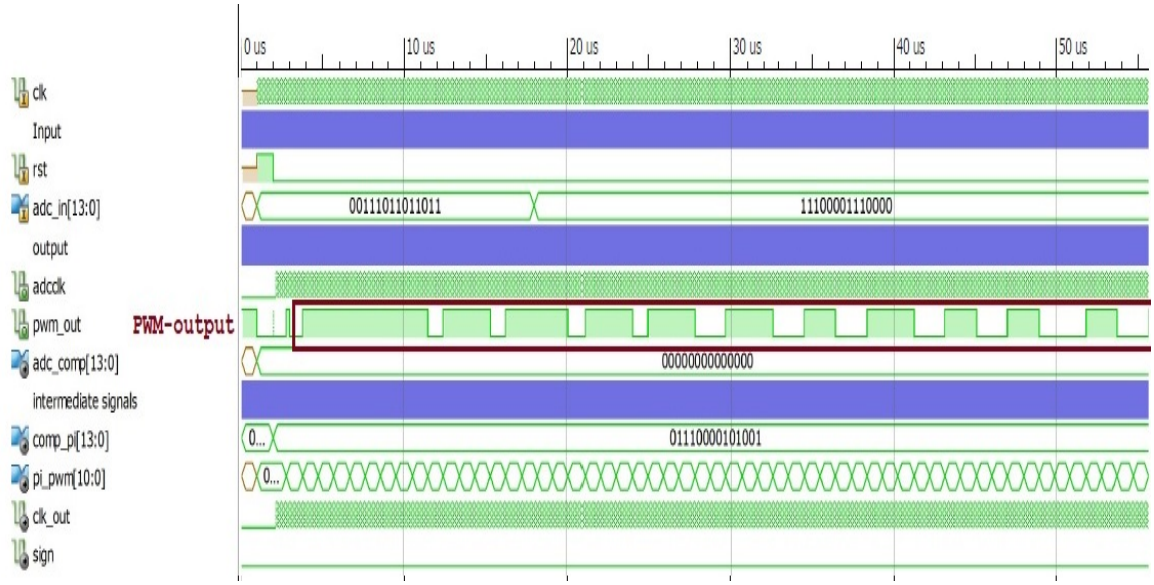

Figure 5.18: Feedback loop Simulation

Real time simulation is carried out using a Logic Analyser inbuilt in the Design suite. ChipScope Pro Logic Analyser is used to debug the feedback path of the Converter. It allows a designer to insert a Integrated Logic Analyser (ILA) core in the design for debugging. The ILA core is a customizable logic analyzer core that can be used to monitor the internal signals in the design. Because the ILA core is synchronous to the design being monitored, all design clock constraints applied to the design are also applied to the components inside the ILA core. With this the output of the PWM generated was tested for different values of input voltage. The real time simulation of the feedback loop for 1.9V of ADC input is shown in figure 5.19. The signal IBUF are the 14 bit ADC converted digital values. The analyzer is sensitive to the changes in the analog signal which can be seen by the toggling of the signals.

The PWM output is a steady signal.

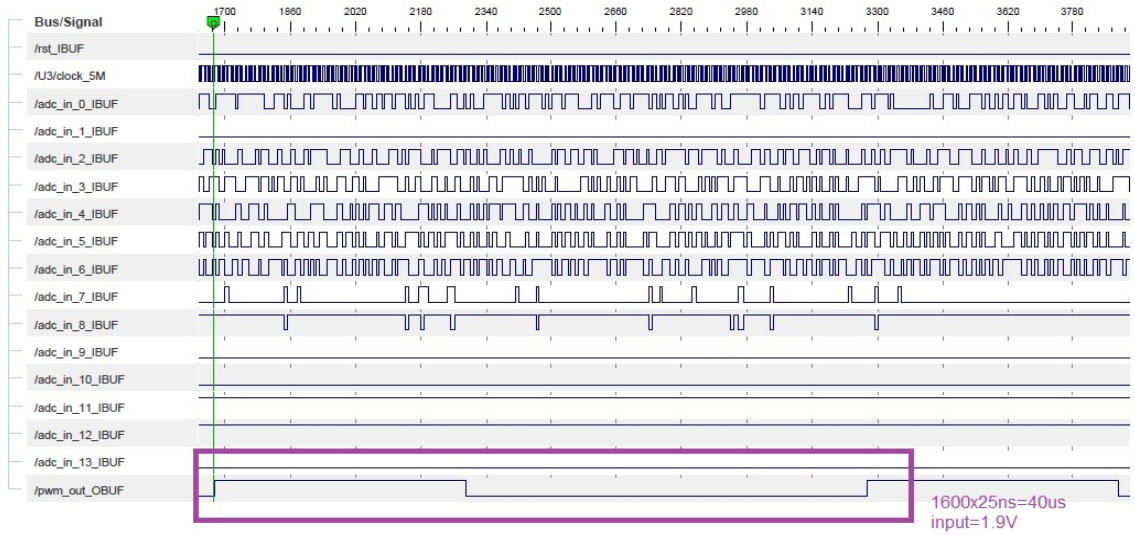

Figure 5.19: Real Time Simulation on Chipscope Logic analyzer for ADC input 1.9 V

Figure 5.20 shows the output for analog input=2.9V. The pulse width is modulated accordingly to the input.

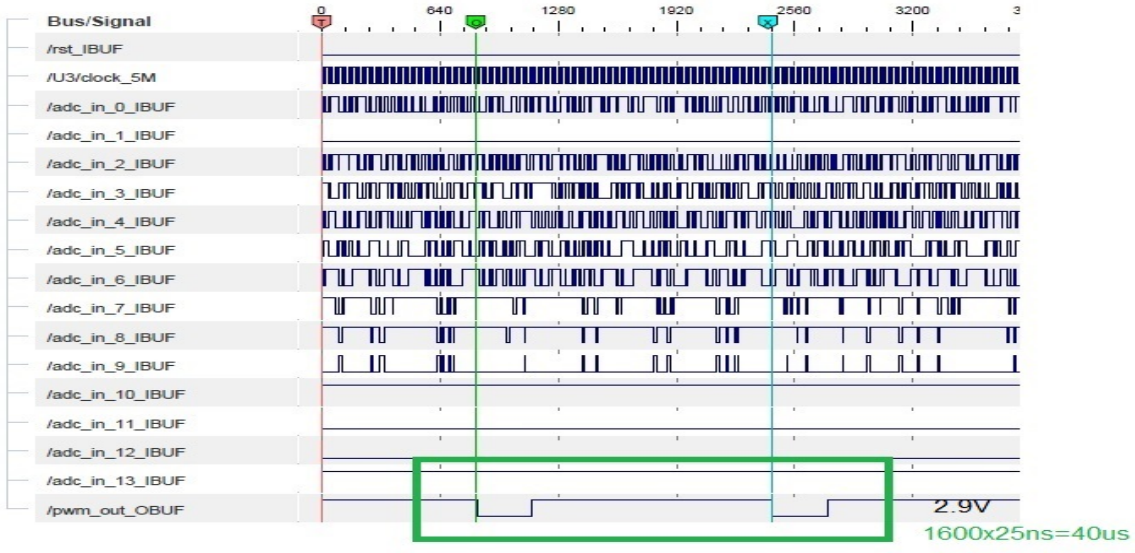

Figure 5.20: Real Time Simulation on Chipscope Logic analyzer for ADC input 2.9 V

5.8 PID Controller

PID Controller is a combination of proportional, integral and derivative control. Derivative mode improves stability of the system and enables increase in gain and decrease in integral

time constant Ti, which increases speed of the controller response.

The structural PI controller is modified to structural PID controller. The discrete equation of PID controller are as follows

$$u(k) = q_0 e(k) + q_1 e(k-1) + q_2 e(k-2) + u(k-1) \tag{5.10}$$

$$q_0 = K_p(1 + \frac{T_s}{T_i} + \frac{T_d}{T_s}) \tag{5.11}$$

$$q_1 = -K_p(1 + 2T_d/T_s) \tag{5.12}$$

$$q_2 = K_p T_d/T_s \tag{5.13}$$

The state diagram for the finite state machine is shown in figure5.21. There are five states and three outputs. The outputs are the Multiplexer Select line S1S0, the output to the accumulator register (accreg) and Final register (finreg) which enables the register to store values. At any stage, if reset is set as 1, then all the register output is set to '0' and process does not start. Once the rst signal is set as '0', the flow shifts to state S1, the multiplexer select lines are set to "00" and accureg is set as 1 while the finareg still remains 0. State S1 is the state for q_0 multiplied with error e(k). In the next clock cycle, i.e. State S2 the select lines are set to "01" and accureg and finalref remain in their previous state.State S2 is the state for q_1 multiplied with the delayed error e(k-1). Similarly in State S3, the select lines are set to "10" and the register signals remains same.State S3 is the state for q_1 multiplied with the delayed error e(k-2). In state S4, the select lines are again set to not defined state, accureg is set '0' and finreg is set to '1'. State S4 is state where the equation is added and the final value is obtained at the output. After this, the entire cycle repeats itself.

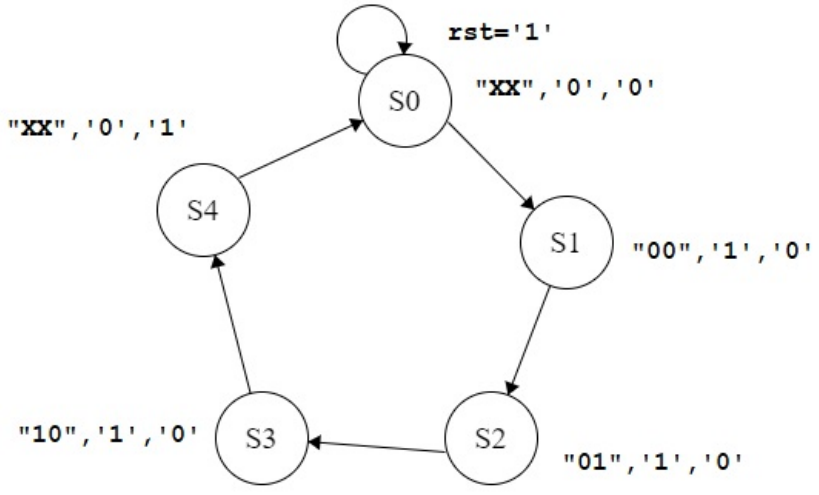

Figure 5.21: Finite state machine for PID controller

The sequence of events is shown in table 5.5

Table 5.5: FSM sequence for PID controller

State	Event	FSM Signals			
		Reset	sel	accreg	finreg
S0	RESET	1	XX	0	0
S1	$q_0 * e(k)$	0	00	1	0
S2	$q_1 * e(k-1)$	0	01	1	0
S3	$q_2 * e(k-2)$	10	1	1	0
S4	OUTPUT	0	XX	0	1

The block diagram of the PID controller is shown in figure 5.22. The top multiplexer 3to1 takes in the error signal e(k),e(k-1) and e(k-2) and the bottom 3:1 multiplexer takes in the PID constants. The Controller generates 3 signals. Signal SEL for the Multiplexer selection, signal accreg for accumulation of register value after addition and the finreg for the final saturated output. The sign bit is checked in the adder and accordingly the control signal is calculated.

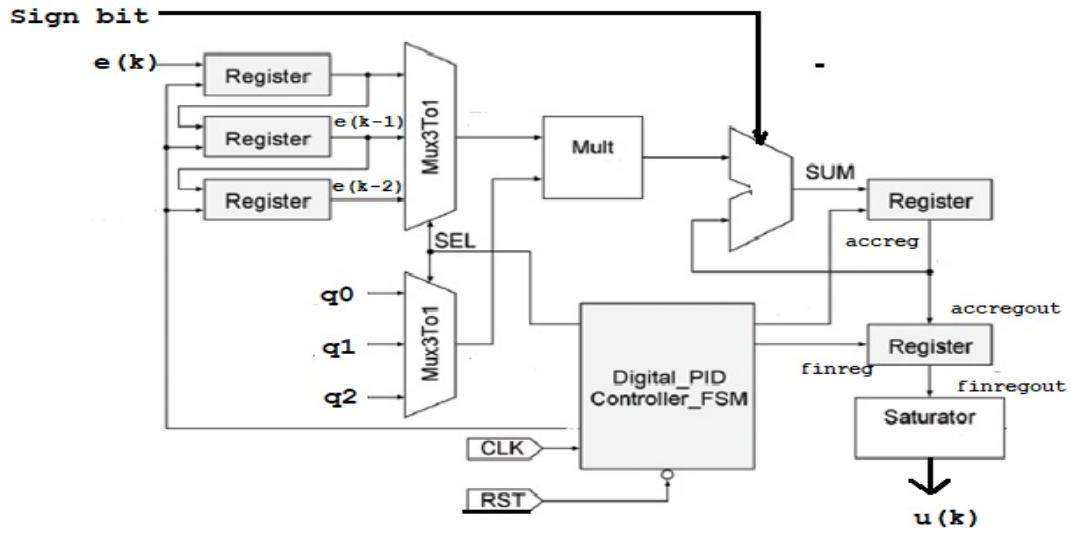

Figure 5.22: Block diagram of PID controller

PID VHDL code is written and synthesized in Xilinx 14.7 ISE Design Suite. The RTL synthesis is as shown in figure 5.23. The 3 registers generate the error signal and their delayed signals, multiplier multiplies the constants, the adder block adds the three terms and

the saturator saturates the output. Clock, reset, sign bit and the error signal are the inputs and the control signal is the output.

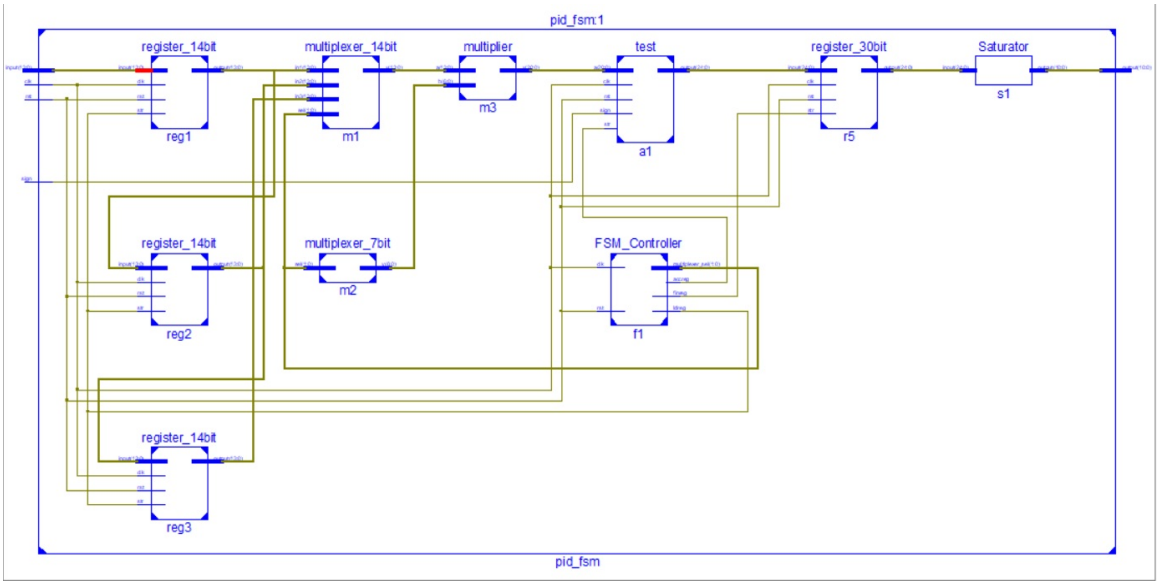

Figure 5.23: PID FSM Synthesis

The PID controller is simulated with other blocks in the feedback loop. The adc value is simulated and the pwm output is observed using ISim simulator. The simulation is shown in figure 5.24

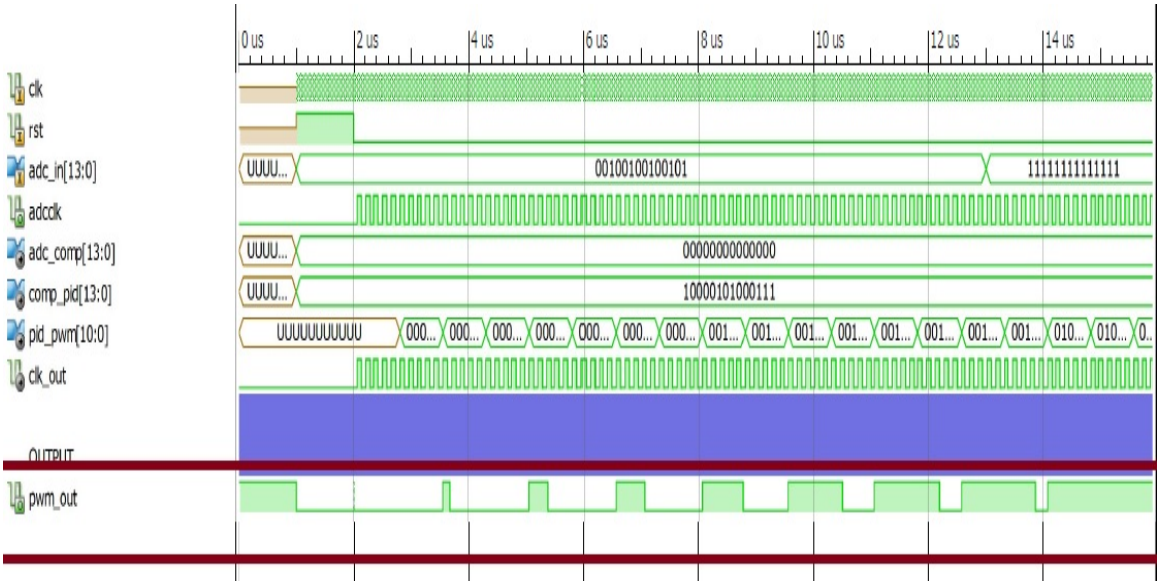

Figure 5.24: Feedback loop Simulation with PID controller

The hardware count of PID controller is shown in table 5.6 It has the registers, multiplier, adder subtractor and the multipler blocks. It also infers a Finite state machine of 5 states.

Table 5.6: Device utilization for PI controller FSM

Cell usage	PID FSM Proposed design	Multiplier based Paper no. [19]
FSM states	5	-
14x7-bit multiplier	1	-
25 bit addsub	1	-
1 bit register	2	-
14-bit register	3	-
2 bit register	1	-
25-bit register	4	-
14-bit 4to1 multiplexer	1	-
No. of slice flipflops	112	268
No.of slice LUT	60	432

5.9 Conclusion

FPGA based control is designed and implemented on a Xilinx FPGA. The blocks of the control feedback loop are design and implemented on FPGA platform using VHDL. The ADC is interfaced with FPGA to sense the voltage from the output of the converter. PI controller is modeled using behavioral, structural and FSM modeling. All three modeling structures are compared for the synthesis and hardware. Simulation is carried out using ISim simulator. Chip Scope is used for Real time Analysis and output of the implemented control loop is validated for different inputs of analog values. PID controller is designed using FSM and verification of the output is carried out. Finally a top level model is built for the feedback loop . The input is the analog output of the controller and the output is the PWM switching signal. The hardware count for PI and PID controller is determined. The PID controller has 112 slice flipflops and 60 number of 4 input LUT which is less as compared to a multiplier based design. Overall the FSM structure gives a better stability to the control loop. The buck and boost converters are tested with the FSM based PI and PID controllers.

Chapter 6

Chaos and Bifurcation Analysis

6.1 Introduction

Non-linearity is present in power electronic circuits because of switching devices, power, passive components, and parasitic effects. This in turn leads to changes in the topology of the devices. The non-linearities cause chaos and bifurcation and make the system unstable. Prediction of these problems helps in preventing the operation of DC-DC converters in the region of non-linearities. Chaos is a state of disorder that is an unforeseeable long-term evolution occurring in a non-linear dynamic system. Small changes in the input will lead to large disturbances in the output. It starts with the appearance of sub harmonics and progresses to chaos. Changing a system parameter leads to a qualitative change in the system dynamics called bifurcation.

It implies the loss of stability of the circuit. The operation of the system goes from a stable region to an unstable region due to changes in the output parameter.

In this chapter, an analysis of chaos is carried out to obtain the bifurcation diagrams for buck and boost converters. The iterative map models are obtained and simulated. The programs are written in Matlab and bifurcation plots are obtained for changes in input voltage and reference current. The models are simulated in Matlab-Simulink to observe the changes in the system parameters in the nonlinear regions of operation.

6.2 Bifurcation and Chaos

Bifurcation theory was originally developed by Poincare to indicate the qualitative change in system behavior, under the variation of one or more parameters on which the system de-

pends. In bifurcation theory, the system variables are defined as state variables and control parameters. The relationship between a control parameter and a state variable is called the state-control space. The locations at which bifurcations occur within the space are called bifurcation points. Bifurcations of fixed-point solutions are classified as static and dynamic bifurcations. Examples of static bifurcation are saddle-node, pitchfork, or transcritical bifurcations. Dynamic bifurcations are also known as Hopf bifurcations. They exhibit periodic solutions. With fixed-point solutions, the local stability of the system is determined from the eigenvalues of the Jacobian matrix of the linearized system. Floquet theory is used for determining the system's stability with periodic solutions. The eigenvalues of the Monodromy matrix are called Floquet or characteristic multipliers. The types of bifurcation are determined from the manner in which the Floquet multipliers leave the unit circle [52]. There are three possible ways for this to happen

i) If the Floquet multiplier leaves the unit circle through +1, then three possible bifurcations may occur: transcritical, symmetry-breaking, or cyclic-fold bifurcation.

ii)A period-doubling (Flip bifurcation) occurs if the Floquet multiplier leaves the unit circle through -1.

iii) If the Floquet multipliers are complex conjugate and leave the unit circle from the real axis, the system exhibits secondary Hopf bifurcation.

A nonlinear system can have a complicated steady-state behavior which is referred as Chaos. The behavior does not have equilibrium or periodic oscillations. Despite the deterministic nature of the system, it is observed that the chaotic motion exhibit randomness.

6.3 Analysis of Buck converter

Analysis of buck converter for chaos and bifurcation is placed with a current controlled model as shown in figure 6.1. All the components are assumed to have ideal characteristics. Each switching cycle starts with the switch S in off condition where t= nT, T is the switching period. Inductor current will start decreasing when switch is off and reach a value equal to I_{ref}. The switch S is turned on when $i_L = I_{ref}$ and will remain in turn-on state until the end of this switching cycle. The advantage of this control mode is that the inductor current is always having a minimum value of I_{ref} and hence always acts in the continuous conduction mode. Considering inductor current i_L and capacitor voltage V_C as state variables, the differential

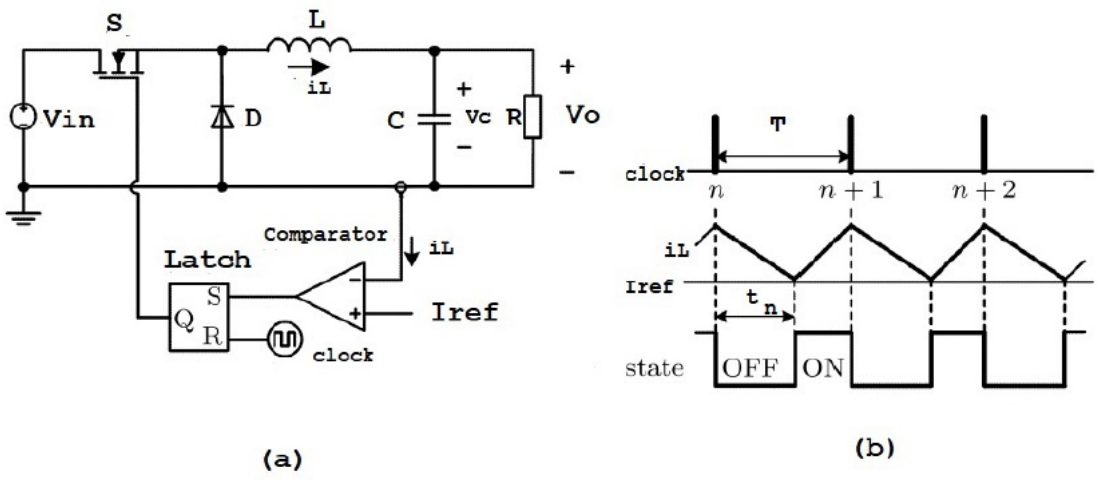

Figure 6.1: Current controlled buck converter (a)Schematic (b)waveforms

equations for the converter during turn on and turn off of the switch are obtained.

When the switch S is ON, the inductor current and capacitor voltage is given by

$$\frac{di_L}{dt} = \frac{V_{in}}{L}\frac{-V_c}{L} \tag{6.1}$$

$$\frac{dV_c}{dt} = \frac{i_L}{C} - \frac{V_c}{RC} \tag{6.2}$$

When the switch is OFF, the inductor current and capacitor voltage is given by

$$\frac{di_L}{dt} = \frac{-V_c}{L} \tag{6.3}$$

$$\frac{dV_c(t)}{dt} = \frac{i_L}{C} - \frac{V_c}{RC} \tag{6.4}$$

6.3.1 Discrete iterative map of buck converter

Discrete time map of DC-DC converters is widely used in iterative mapping. The state variable i_L and V_c are periodically sampled at time instances t= nT. This model is obtained by increments. The aim is to derive the iterative function that expresses the state variables at one sampling instant in terms of earlier sampling instant [52] [59]. The initial condition of state variables are 'n' at the starting and 'n+1' after completing one switching cycle. The state variables for initial and final conditions are given by $i_n$and V_n and $i_{n+1}$and V_{n+1} respectively.

The turn-off time for the n^{th} switching cycle is obtained as from equation 6.1 as

$$t_n = \frac{L}{V_n}(i_n - I_{ref}) \tag{6.5}$$

For CCM mode, the parameters of buck converter should satisfy $L < 4R^2C$

The capacitor voltage at t=nT+t_n is obtained by solving equation 6.1 and equation 6.2

$$V_c(t_n) = e^{(-kt_n)}(V_n cos(wt_n) + (\frac{i_n}{wC} - \frac{k}{w}V_n)sin(wt_n)) \tag{6.6}$$

where k=$\frac{1}{2RC}$ and ω=$\sqrt{\frac{1}{LC} - k^2}$

The iterative map model is derived for two cases.

Case1: t_n> T The switch will be OFF and the iterative map is given by

$$i_{n+1} = e^{(-kt_n)}[i_n cos(wT) + (\frac{K}{w}i_n - \frac{1}{wL}V_n)sin(wT)] \tag{6.7}$$

$$V_{n+1} = e^{(-kt_n)}[V_n cos(wT) + (\frac{i_n}{wC} - \frac{k}{w}V_n)sin(wT)] \tag{6.8}$$

Case2: t_n<T The switch S will be ON and the iterative map is given by

$$i_{n+1} = e^{(-k(T-t_n))}[C_1 cos(w(T-t_n)) + C_2 sin(w(T-t_n))] + \frac{V_{in}}{R} \tag{6.9}$$

$$V_{n+1} = e^{(-k(T-t_n))}[C_3 cos(w(T-t_n)) + C_4 sin(w(T-t_n))] + V_{in} \tag{6.10}$$

where C_1, C_2, C_3, C_4 are constants

$$C_1 = I_{ref} - \frac{V_{in}}{R}$$

$$C_2 = \frac{k}{w}C_1 + \frac{V_{in} - V_c(t_n)}{wL}$$

$$C_3 = V_c(t_n) - V_{in}$$

$$C_4 = \frac{k}{w}C_3 + \frac{I_{ref} - V_c(t_n/R)}{wC}$$

The iterative model is simulated using a Matlab code and the variation in input voltage and reference current versus inductor current is observed. A phase portrait is a view of state space with the state variables as coordinates. The state of the system at any instant is represented by a point in phase plane. The movement of the point is determined by the state equations.

6.3.2 Simulations for buck converter

The Matlab code is simulated for constant reference current. The specifications are L=2.4mH, C=50 uF, Vin=24V, Vout =12V and Iref=2A. The inductor current and capacitor voltage are

the state variables and at each state ‘n’ the present values are fed back to get the new values at ‘n+1’ [60]. Figure 6.2 shows the discrete iterative map of the buck converter simulated for n=100. It can be seen that the buck converter has a steady output current of 2.05A till Vin = 25V represented as ‘A’. This represents orbit 1 operation. It then goes into orbit 2 represented by ‘B’at 26V. Further it goes into chaos region shown by ‘C’. The inductor current is analyzed for the three input voltages 24V, 26V and 30V. Figure 6.3 shows inductor current at 2A for a sample size of 30 points. It settles down to a constant value and there is a steady behavior. Figure 6.4 is simulated for Vin = 26V representing orbit 2. the inductor value also has 2 values oscillating. Figure 6.5 shows the inductor value for input voltage Vin = 30V . The output is random and non linear depicting the chaos region.

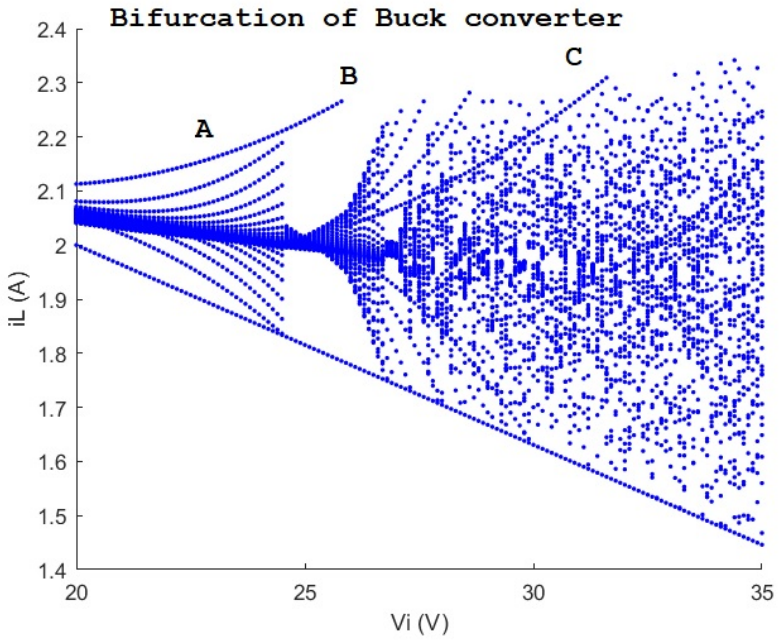

Figure 6.2: Bifurcation diagram for Buck converter for i_L with V_{in} as a control parameter (I_{ref}=2A)

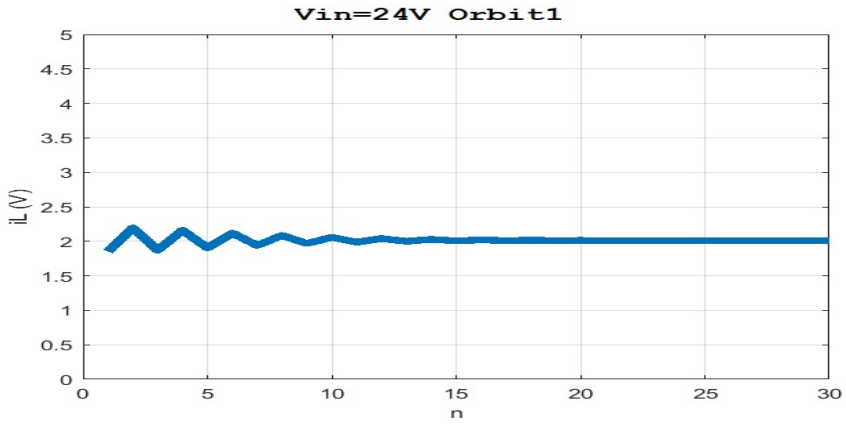

Figure 6.3: Inductor current for Vin=24V

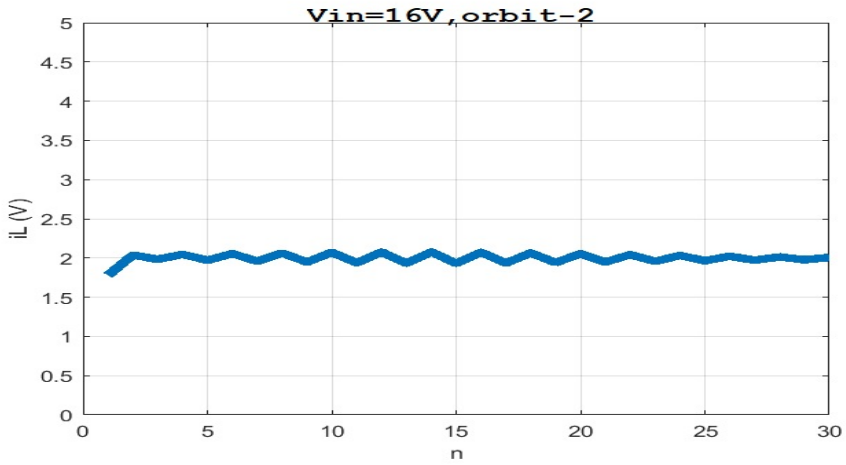

Figure 6.4: Inductor current for Vin=26V

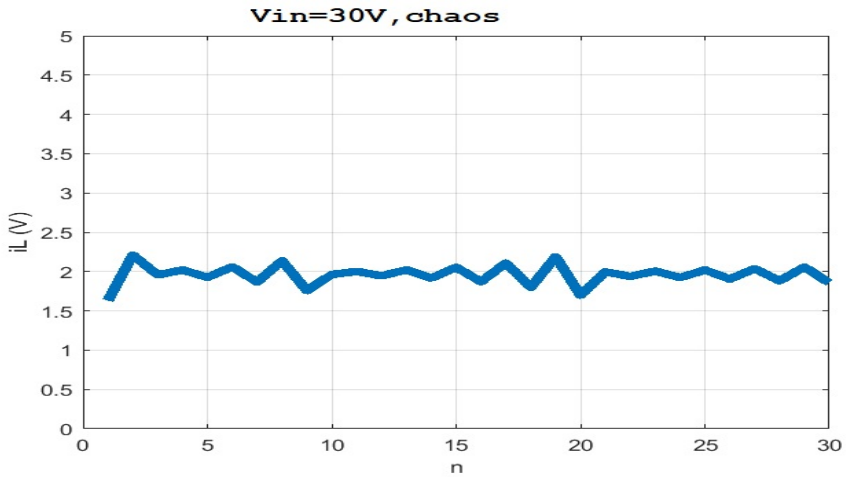

Figure 6.5: Inductor current for Vin=30V

6.4 Analysis of boost converter

A circuit diagram for a boost converter is shown in figure 6.6. The switch is controlled by a

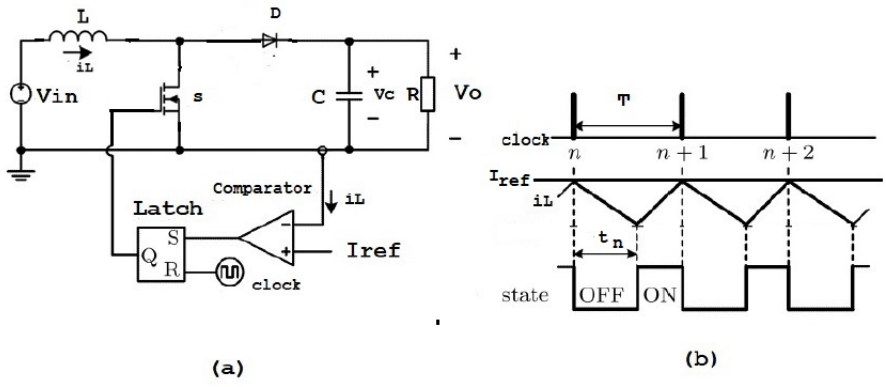

Figure 6.6: Current controlled boost converter (a)Schematic (b)waveforms

current feedback path consisting of a comparator and a flip-flop. The repetitive clock pulse sets the flip-flop, which turns on the switch. The inductor current increases, storing energy in the magnetic field of the inductor. When the inductor current reaches the reference value, the comparator resets the flip-flop, which turns-off the switch. As a result of Lenz's law, a voltage is induced in the inductor, in such a direction as to try to maintain the current flow. This forward biases the diode D and energy is transferred from the inductor to the capacitor and the load. The magnitude of the reference current determines the amount of energy transferred from the input to the output of the converter and consequently the magnitude of the converter output voltage for a given load resistance. Considering inductor current i_L and capacitor voltage V_C as state variables, the differential equations for the converter during turn on and turn off of the switch are obtained.

6.4.1 Discrete iterative map of boost converter

Discrete time map of DC-DC converters is widely used in iterative mapping. The state variable i_L and V_c are periodically sampled at time instances t= nT This model is obtained by increments [59]. The aim is to derive the iterative function that expresses the state variables at one sampling instant in terms of earlier sampling instant.

The initial condition of state variables are 'n' at the starting and 'n+1' after completing one switching cycle. The state variables for initial and final conditions are given by $i_n$and V_n and $i_{n+1}$and V_{n+1} respectively.

When the switch S is ON, the inductor current and capacitor voltage is given by

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{6.11}$$

$$\frac{dV_c}{dt} = -\frac{V_c}{RC} \tag{6.12}$$

The inductor current i_L in iterative map is i_n at time t=0 and I_{ref} at t=t_n. From equation6.11

$$t_n = \frac{L}{V_{in}}(I_{ref} - i_n) \tag{6.13}$$

Capacitor voltage V_n at t=0, the solution of equation 6.12 at t=t_n is

$$V_c(t_n) = V_n e^{-\frac{t_n}{\tau_{RC}}} \tag{6.14}$$

where the time constant τ_{RC} =RC and t_n is the time when switch is open.

When the switch is OFF, the inductor current and capacitor voltage is given by

$$\frac{di_L}{dt} = \frac{V_{in}}{L} - \frac{Vc}{L} \tag{6.15}$$

$$\frac{dV_c(t)}{dt} = \frac{i_L}{C} - \frac{V_c}{RC} \tag{6.16}$$

From equation6.15 and 6.16 , a differential equation is obtained

$$\frac{d^2 i_L}{dt^2} + \frac{1}{RC}\frac{di_L}{dt} + \frac{1}{LC} i_L = \frac{V_{in}}{RLC} \tag{6.17}$$

The solution of differential equation 6.17 comprises of a homogeneous solution and particular solution. The particular solution is obtained by assigning the constant value to i_L in 6.17 thereby having

$$i_{L_p}(t) = \frac{V_{in}}{R} \tag{6.18}$$

The general solution is given by

$$i_L(t) = e^{-kt}(A_1 sinwt + A_2 coswt) + \frac{V_{in}}{R} \tag{6.19}$$

A_1, A_2 are boundary conditions where k=$\frac{1}{2\tau_{RC}}$ ω=$\sqrt{\frac{1}{LC} - k^2}$

Equation 6.19describes the current till the closing of the switch at time $t_n^{'}$ where

$$t_n{}' = T[1 - (\frac{t_n}{T})] \tag{6.20}$$

at t=0, A_2 is obtained

$$A_2 = I_{ref} - \frac{V_{in}}{R} \tag{6.21}$$

Using equation6.19 and differentiating at t=0, solving for A_1

$$A_1 = \frac{kLI_{ref}^{'} + V_{in} - V_n e^{-t_n/\tau_{RC}}}{wL} \tag{6.22}$$

where

$$I_{ref}^{'} = I_{ref} - \frac{V_{in}}{R} \tag{6.23}$$

Substituting equation 6.21 and 6.22 in 6.19 gives the value of i_{n+1} the next state of the inductor current

$$i_{n+1}(t) = e^{-kt_n^{'}}[(\frac{kLI_{ref}^{'} + V_{in} - V_n e^{-t_n/\tau_{RC}}}{wL})sinwt_n^{'} + (I_{ref} - \frac{V_{in}}{R})coswt_n^{'}] + \frac{V_{in}}{R} \tag{6.24}$$

A similar mathematical approach to equation6.15 and 6.16 in terms of capacitor voltage V_c give the differential equation as

$$\frac{d^2V_c}{dt^2} + \frac{1}{RC}\frac{dV_c}{dt} + \frac{1}{LC}V_c = \frac{V_{in}}{LC} \tag{6.25}$$

The general solution is given by

$$V_c(t) = e^{-kt}(B_1 sinwt + B_2 coswt) + V_{in} \tag{6.26}$$

Applying the boundary conditions, B_1 and B_2 are obtained and the next state capacitor voltage is given by

$$V_{n+1}(t) = e^{-kt_n^{'}}[(KV_n e^{-t_n/\tau_{RC}} - kV_{in} - \frac{I_{ref}^{'}}{C})\frac{sinwt_n^{'}}{w} + (V_{in} - V_n e^{-t_n/\tau_{RC}})coswt_n^{'}] \tag{6.27}$$

Equations 6.24 and 6.27 are simulated in Matlab code to obtain the bifurcation diagrams.

6.4.2 Simulations for boost converter

A matlab code is written to obtain the bifurcation diagrams. The boost converter is designed and has the following specifications Vin=5V, Vout=10V, I=2A, f=50KHz, L=5mH, C=20uF, R=10Ohms.

The Matlab code is written for which the algorithm is shown in figure 6.7. The bifurcation diagrams are constructed to obtain the variation of inductor current with the changes in input voltage and changes in reference current [59].

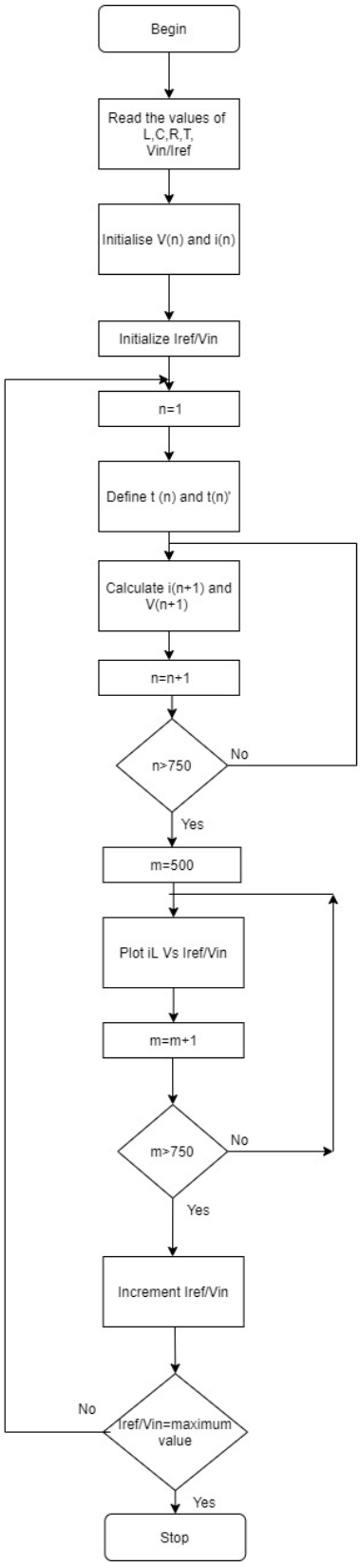

Figure 6.7: Flowchart for bifurcation

Referring to the flowchart in figure 6.7 , the current state is i(n) and V(n) and the next state is i(n+1) and V(n+1) where i and V are the inductor currents and capacitor voltages

respectively. Equations 6.24 and 6.27 were iterated 750 times. The first 500 iterations were discarded, to eliminate transient conditions and the last 250 were plotted. Figure 6.8 shows the bifurcation of inductor current with respect to changes in input voltage. The chaotic region is seen from V_{in} =1V to 4.5V. A doublet is seen from 4.5V to 6.5V. Beyond this region, the converter is having a stable region.

Figure 6.9 shows the bifurcation of capacitor voltage with respect to changes in input voltage. Three reference points A,B,C are considered for input voltage 8V, 5.5V and 3.5V respectively. These voltages are taken in the stable region, doublet and chaos regions. A boost converter model is simulated in Matlab simulink and the outputs are verified for the mentioned three points. Figure 6.10 shows the output in the stable region for input voltage V_{in} = 8V. It shows uniform output. Figure 6.11 shows the output voltage for input voltage V_{in} = 5.5V in the doublet region point B. The output voltage is having a smaller peak in between two larger peaks. Figure 6.12 shows the output waveform for the chaotic region C for input voltage 3.5V wherein the waveform is distorted .

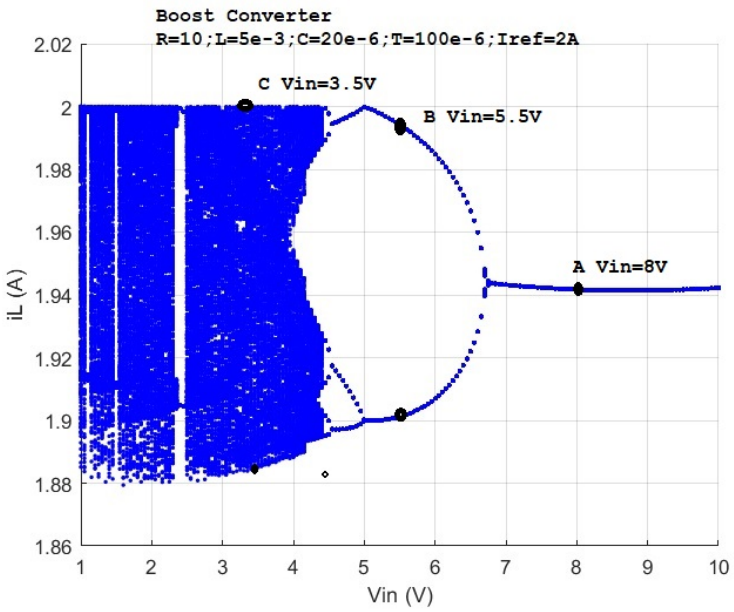

Figure 6.8: Bifurcation diagram for i_L with V_{in} as a control parameter (I_{ref}=2A)

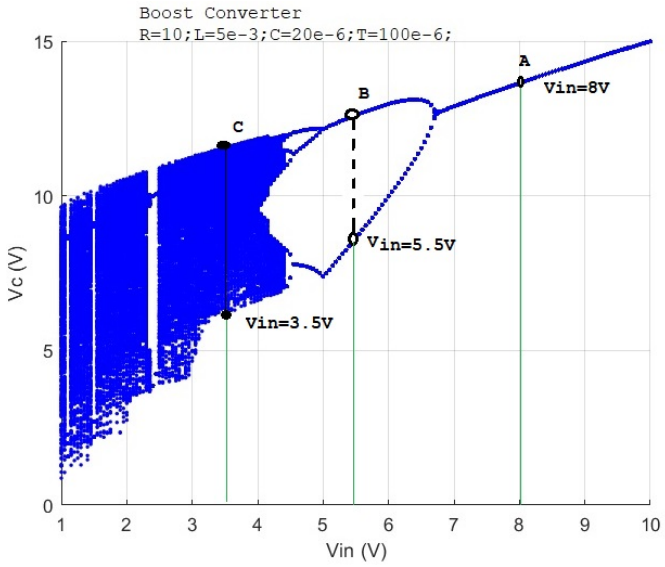

Figure 6.9: Bifurcation diagram for V_c with V_{in} as a control parameter (I_{ref}=2A)

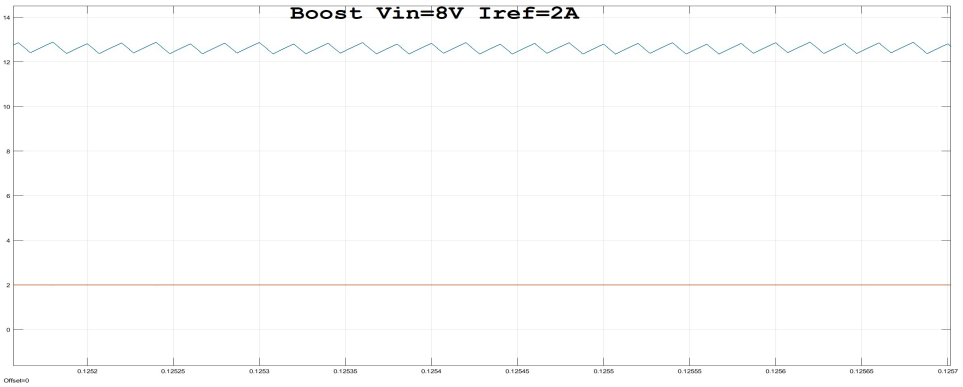

Figure 6.10: Simulink output for the Output Voltage for V_{in} =8V

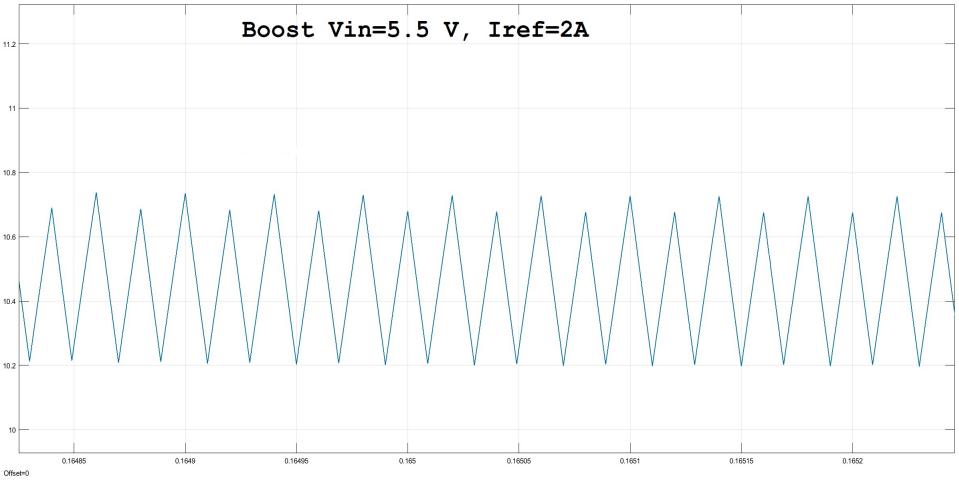

Figure 6.11: Simulink output for the Output Voltage for V_{in} =5.5V

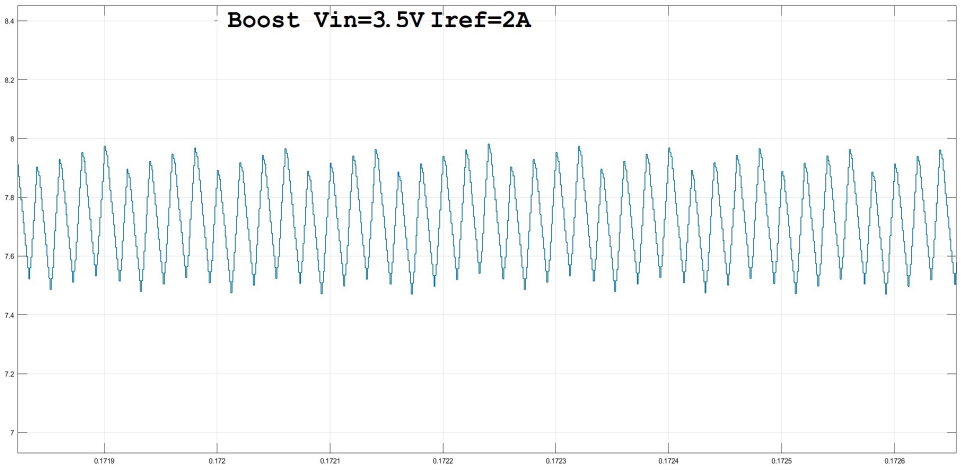

Figure 6.12: Simulink output for the Output Voltage for V_{in} =3.5V

The variation of inductor current with reference current as the control parameter is shown in figure 6.13. The system is period-I and inductor current has a single value till I_{ref} =0.8A. The system displays period-2 as one of the Floquet multipliers leaves the unit circle through -1, producing a period-doubling bifurcation. During period-2, the inductor current has two unique values at alternate instants of turn-on. For I_{ref}=1.25 A, the inductor current has two values 0.8A and 1.3A. Further, the system undergoes stable period-3 operation, and eventually becomes chaotic at I_{ref}= 1.5A, with the value at each turn-on having many values. The diagram indicates that the system is stable for lower values of reference current and becomes unstable as it increases.

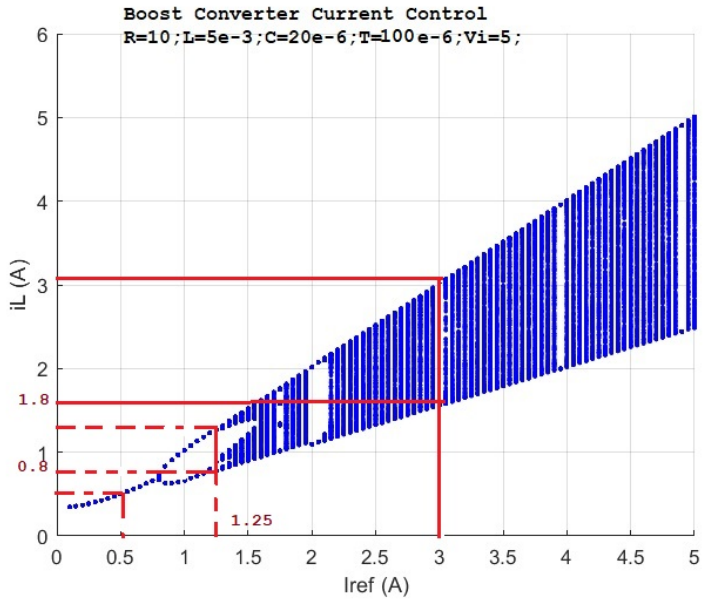

Figure 6.13: Bifurcation diagram for i_L with I_{ref} as a control parameter (V_{in}=5V)

Matlab simulations are performed for various values of reference current and keeping the input voltage constant. The output voltage is observed for the three different values of reference current corresponding to period-1, period-2 and chaos region.

Figure 6.14 is for I_{ref}=0.5A. The output waveform is uniform. Figure 6.15 shows the output voltage for I_{ref}= 1.25A which has one smaller peak between two larger peaks representing the doublet. Figure 6.16 shows the output voltage for the chaos with I_{ref}= 3A. the output is random and non uniform.

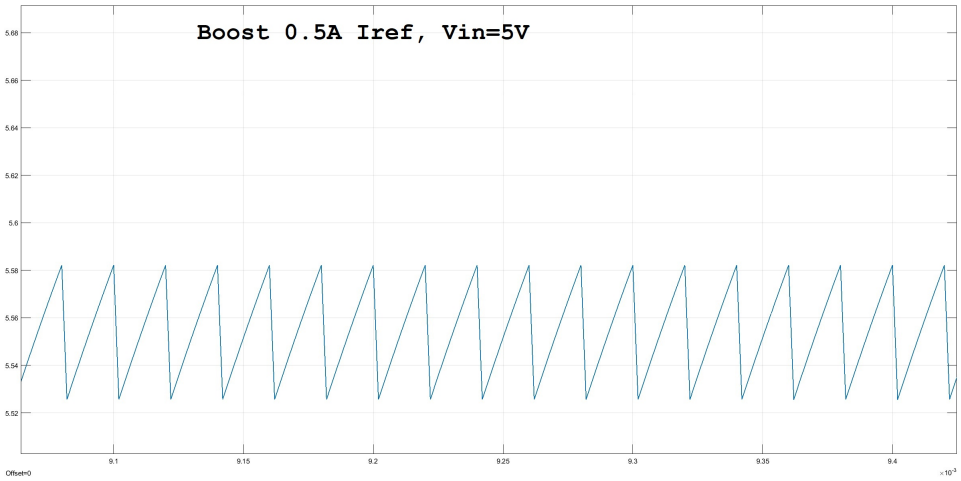

Figure 6.14: Simulink output for the Output Voltage for I_{ref} =0.5A

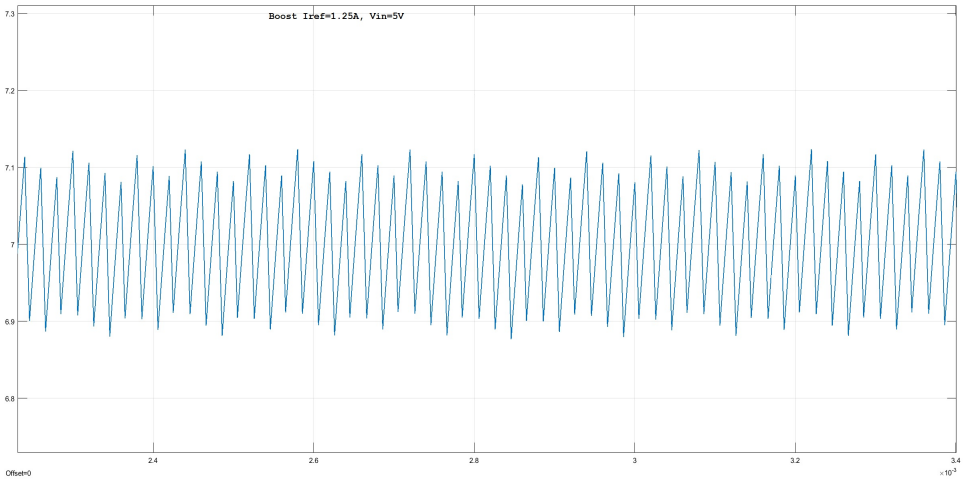

Figure 6.15: Simulink output for the Output Voltage for I_{ref} =1.25A

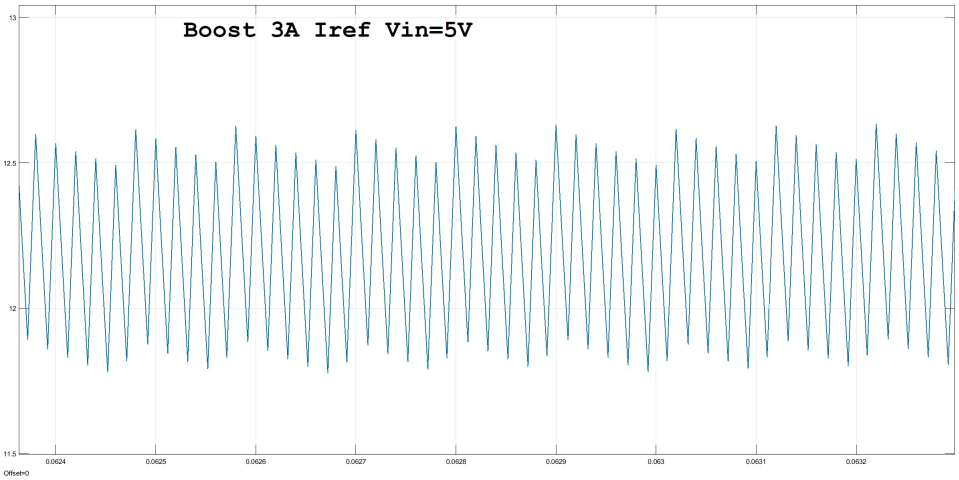

Figure 6.16: Simulink output for the Output Voltage for I_{ref} =3A

6.5 Conclusion

Buck and boost converters are verified for their chaotic operation. The discrete iterative maps for buck and boost converters are modeled. The discrete maps are simulated in Matlab by writing a Matlab code. The bifurcation diagrams are obtained which show the chaotic behavior of the converters for variation in the control signal. Bifurcation diagram is obtained for a buck converter by varying the input voltage and obtaining the inductor current. It is observed that the converter operates in orbit 2 for 26V input voltage and displays a chaotic behavior for a 30V input voltage. Boost converter displays a chaotic behavior for 3.5V input voltage and 1.25A reference current. The output results are verified by simulating the inductor currents for the values of the control signals obtained in the bifurcation diagrams thus validating the iterative maps. The condition at which chaos occurs has been observed so that the system is operated in orbit-1 region i.e the stable region.

Chapter 7

Conclusions and Future work

7.1 Conclusion

Switching converters were modeled, designed and simulations were carried out using Matlab Simulink. They were implemented in hardware and tested for open loop and closed loop control with FPGA based controller. Simulations were performed for buck converter with different compensators viz. PI,lead,PI with lead and PID. Buck converter was analyzed for the frequency and time domain specifications. It was observed that PI controller improves the phase margin from 19.1° to 27.4°. The gain cross over frequency was increased to 1.31 krad/s from 960 rad/s. The PID controller improved the phase margin to 49.2°, and achieved a overshoot of 0.03% and a settling time of 1.5 msec. Hardware implementation of buck converter with a FPGA based PI and PID controller was carried out and the voltage regulation was computed. The closed loop was performed with different values of PI and PID constants and optimal control was obtained. The variation in the output voltage was observed to be 0.1 with PI controller for buck converter. Variation in output voltage was 0.05 for a PID controller. It was observed that the PID controller gave a better voltage regulation as compared to the PI controller. Boost converter hardware with FPGA based controller has also been implemented. The voltage regulation obtained was 0.05. FPGA based controllers were designed using behavioral , structural and finite state machine modeling with VHDL language. Simulations and synthesis was carried out using Xilinx ISE Design suite 14.7. ISim simulator was used for functional simulation.Chip scope pro logic analyzer was used for real time simulations. The feedback loop was designed and implemented on FPGA . Onboard ADC was also interfaced with FPGA using VHDL. Thus the entire feedback loop was successfully implemented and interfaced in real time. Hardware utilized by the logic

was tabulated. It was observed that PID controller with finite state machine modeling generated a reduced hardware as compared to the multiplier based controller. It is concluded that a versatile FPGA based controller for a low frequency DC-DC switching converters was successfully implemented and tested. Analysis of the converters for nonlinear characteristics was performed and the bifurcation diagrams for buck and boost converters were simulated in Matlab. The various regions of bifurcation were validated using Matlab Simulink models. The designed controller and the control loop can be used for all other types of DC-DC converters.

7.2 Future work

The research tested the buck and the boost converters which are the basic converters. Testing of controller with other configurations of DC-DC converters may be carried out with the designed FPGA based controller. The FPGA controller designed for switching converters may be implemented on an Application Specific Integrated Circuit (ASIC). The constants for the controller are defined in the VHDL code. The controller design may be taken up with an external interface for tuning the digital value of the constants. Similarly, the reference value is also set up in the code for the digital comparator. The reference value may also be interfaced externally. The controller design using the FSM modeling may be taken up for non linear controllers. Hardware models for chaos and bifurcations may be created for non linear analysis. Thus, using the designed methodology for FPGA controllers and interfacing strategy with buck and boost converters, appropriate solution may be obtained for closed loop control using FPGA platform for all types of switching converters.

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